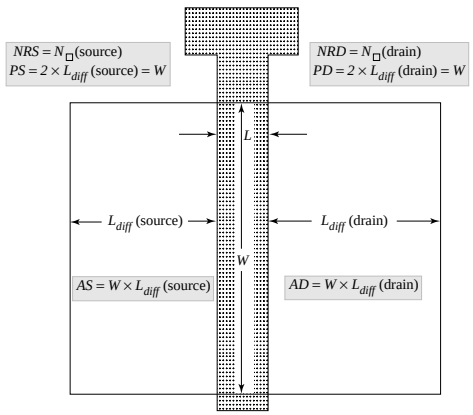
MOSFET Geometry in SPICE

- Statement for MOSFET ... *D,G,S,B* are node numbers for drain, gate, source, and bulk terminals

M*name D G S B MODname* **L= _ W=_ AD= _ AS=_ PD=_ PS=_**

MODname specifies the model name for the MOSFET



MOSFET Model Statement

.MODEL *MODname* **NMOS/PMOS VTO=_ KP=_ GAMMA=_ PHI=_ LAMBDA=_ RD=_ RS=_ RSH=_ CBD=_ CBS=_CJ=_ MJ=_ CJSW=_ MJSW=_ PB=_ IS= _ CGDO=_ CGSO=_ CGBO=_ TOX=_ LD=_**

Parameter name (SPICE / this text)	SPICE symbol Eqs. (4.93), (4.94)	Analytical symbol Eqs. (4.59), (4.60)	Units
channel length	L_{eff}	L	m
polysilicon gate length	L	L_{gate}	m
lateral diffusion/ gate-source overlap	LD	L_D	m
transconductance parameter	KP	$\mu_n C_{ox}$	A/V^2
threshold voltage / zero-bias threshold	VTO	V_{TnO}	V
channel-length modulation parameter	$LAMBDA$	λ_n	V^{-1}
bulk threshold / backgate effect parameter	$GAMMA$	γ_n	$V^{1/2}$
surface potential / depletion drop in inversion	PHI	$-\phi_p$	V

DC Drain Current Equations:

$$I_{DS} = 0 \qquad (V_{GS} \le -V_{TH})$$

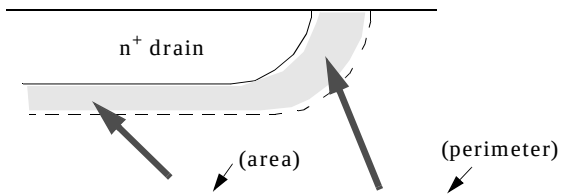
$$I_{DS} = \frac{KP}{2}(W/L_{eff})V_{DS}[2(V_{GS} - V_{TH}) - V_{DS}](1 + LAMBDA \cdot V_{DS}) \qquad (0 \le V_{DS} \le V_{GS} - V_{TH})$$

$$I_{DS} = \frac{KP}{2}(W/L_{eff})(V_{GS} - V_{TH})^2(1 + LAMBDA \cdot V_{DS}) \qquad (0 \le V_{GS} - V_{TH} \le V_{DS})$$

$$V_{TH} = V_{TO} + GAMMA(\sqrt{2 \cdot PHI - V_{BS}} - \sqrt{2 \cdot PHI})$$

Capacitances

SPICE includes the “sidewall” capacitance due to the perimeter of the source and drain junctions --



$$C_{BD}(V_{BD}) = \frac{CJ \cdot AD}{(1 - V_{BD}/PB)^{MJ}} + \frac{CJSW \cdot PD}{(1 - V_{BD}/PB)^{MJSW}}$$

Gate-source and gate-drain overlap capacitance are specified by *CGDO* and *CGSO* (units: F/m).

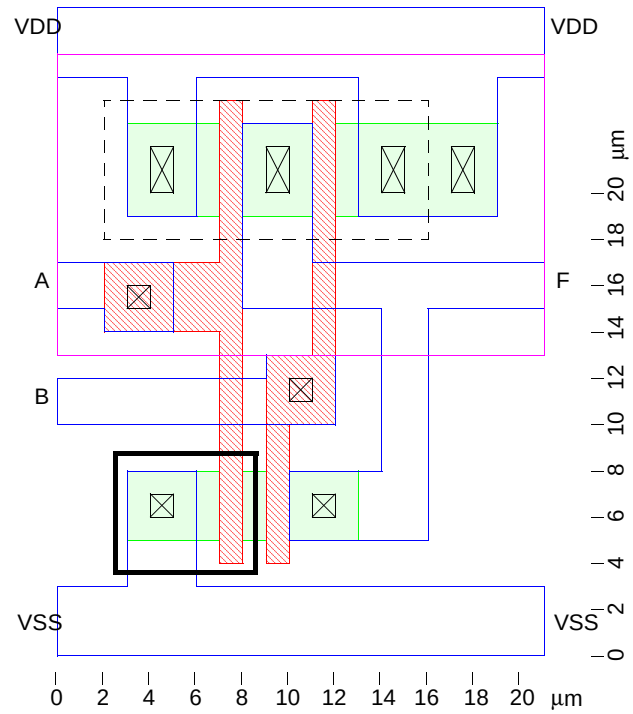
Level 1 MOSFET model:

.MODEL MODN NMOS LEVEL=1 VTO=1 KP=50U LAMBDA=.033 GAMMA=.6
+ PHI=0.8 TOX=1.5E-10 CGDO=5E-10 CGSO= 5e-10 CJ=1E-4 CJSW=5E-10
+ MJ=0.5 PB=0.95

The Level 1 model is adequate for channel lengths longer than about 1.5 µm

For sub-µm MOSFETs, **BSIM** = “Berkeley Short-Channel IGFET Model” developed by Profs. P. Ko (now at HKUST) and C. Hu and their students is the industry-standard SPICE model for MOSFETs.

SPICE Statement for a MOSFET



SPICE Netlist for Extracted Circuit

- Number nodes sequentially; let V_{SS} = 0 , V_{DD} = 5 V, and V_B = 5 V.

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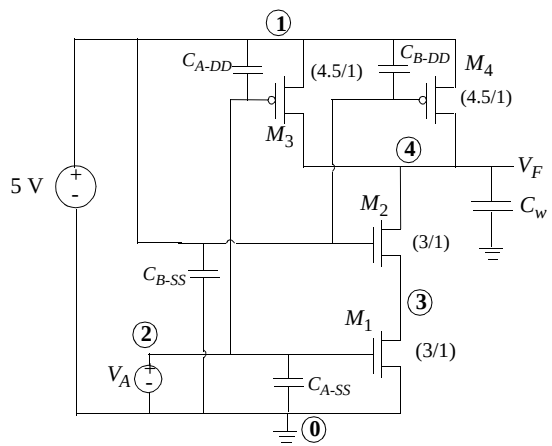


SPICE Input File

- Source File (parastic and load capacitors omitted since the output we want the DC transfer curve and not a transient response)

```
* simple NAND gate
VDD 1 0 5
VA 2 0 DC
M1 3 2 0 0 modn W=3u L=1u AD=3p AS=12p PD=2u PS=10u
M2 4 1 3 0 modn W=3u L=1u AD=12p AS=3p PD=10u PS=2u
M3 4 2 1 1 modp W=4.5u L=1u AD=8p AS=18p PD=2u PS=12.5u
M4 4 1 1 1 modp W=4.5u L=1u AD=8p AS=18p PD=2u PS=12.5u
* standard H&S level 1 models for L = 1 um
.model modn nmos level=1 vto=1 kp=50u lambda=.1 gamma=.6 phi=.8 tox=15e-9
+ cgdo=.5e-9 cgso=.5e-9 cj=.1e-3 cjsw=.5e-9 mj=.5 pb=.95
.model modp pmos level=1 vto=-1 kp=25u lambda=.1 gamma=.6 phi=.8 tox=15e-9
+ cgdo=.5e-9 cgso=.5e-9 cj=.3e-3 cjsw=.35e-9 mj=.5 pb=.89
* dc transfer curve for VA = 0 to 5 V with 0.1 V steps
.DC VA 0 5 0.1
.END
```

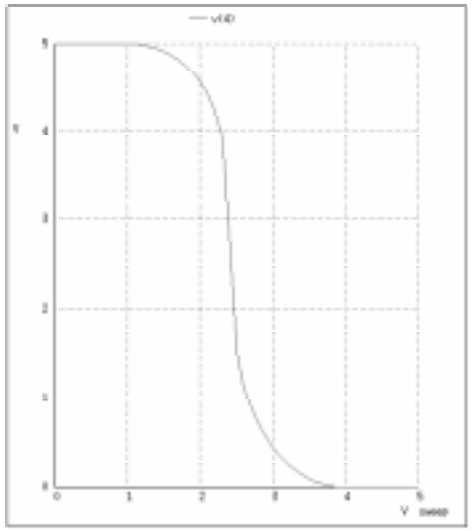
- Spice3 command line syntax

Spice 1 -> load sourcefile

Spice 2 -> run

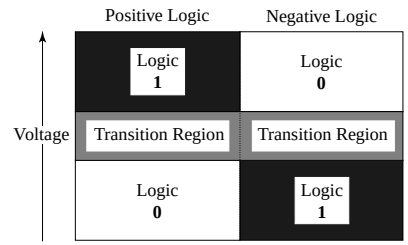
Spice 3 -> plot v(4)

Graphical Output



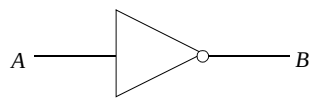
Digital Electronics

- Assign “1” and “0” to a range of voltage (or current), with a separation that minimizes a transition region



We will use positive logic (usually the case)

Simplest binary function: inversion



A	*B*
0	1
1	0

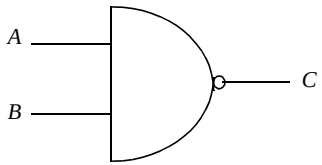
Circuit must take the “1” voltage range at the input and deliver the “0” voltage range at the output.

Boolean Algebra

- Standard logic functions

NAND (not AND) gate

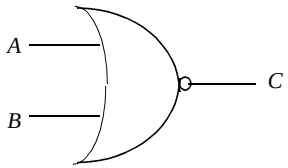
$C = \overline{AB}$



A	B	AB	C

NOR (not OR) gate

$C = \overline{A+B}$

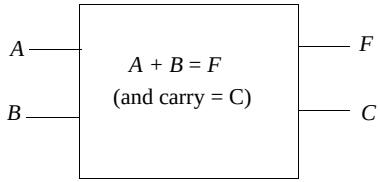


A	B	$A+B$	C

Boolean Algebra

- Adding two-digit binary numbers:

  Truth table



A	B	F	C

Synthesis using standard NAND and NOR gates: $C = AB$, $F = A \otimes B$ (XOR)