(Saturated) MOSFET Small-Signal Model

- Concept: find an equivalent circuit which interrelates the incremental changes in $i_D, v_{GS}, v_{DS}$ etc. for the MOSFET in saturation.

\[ v_{GS} = V_{GS} + v_{gs}, \quad i_D = I_D + i_d \rightarrow \text{we want to find } i_d = (\cdot) v_{gs} \]

We have the functional dependence of the total drain current in saturation:

\[ i_D = \mu_n C_{ox} \left( \frac{W}{2L} \right) \left( v_{GS} - V_{Tn} \right)^2 \left( 1 + \lambda_n v_{DS} \right) = i_D(v_{GS}, v_{DS}) \]

Solution: do a Taylor expansion around the DC operating point (also called the quiescent point or $Q$ point) defined by the DC voltages $Q(V_{GS}, V_{DS})$:

\[ i_D = I_D + \frac{\partial i_D}{\partial v_{GS}} \bigg|_Q (v_{gs}) + \frac{1}{2} \frac{\partial^2 i_D}{\partial v_{GS}^2} \bigg|_Q (v_{gs})^2 + \cdots \]

If the small-signal voltage is really "small," then we can neglect all everything past the linear term --

\[ i_D = I_D + \frac{\partial i_D}{\partial v_{GS}} \bigg|_Q (v_{gs}) = I_D + g_m v_{gs} \]

where the partial derivative is defined as the transconductance, $g_m$.

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Transconductance

The small-signal drain current due to $v_{gs}$ is therefore given by

\[ i_d = g_m v_{gs} \]
Another View of \( g_m \)

* Plot the drain current as a function of the gate-source voltage, so that the slope can be identified with the transconductance:

\[
\begin{align*}
V_{GS} &= 3 \text{ V} \\
V_{DS} &= 4 \text{ V}
\end{align*}
\]

\[ i_D = I_D + i_d \]

\[ V_{GS} = V_{GS} + v_{gs} \]

\[ V_{DS} = 4 \text{ V} \]

\[ \mu_n C_{ox} \frac{W}{L} \]

\[ V_Tn \]

\[ \lambda_n V_{DS} \]

\[ V_{GS} - V_{Th} \]

\[ I_D \]

\[ g_m = \frac{\mu_n C_{ox}}{V_Tn} \left( V_{GS} - V_{Th} \right) (1 + \lambda_n V_{DS}) \]

\[ g_m = \left[ 2 \mu_n C_{ox} \left( \frac{W}{L} \right) I_D \right]^2 \frac{V_{GS} - V_{Th}}{V_{GS} - V_{Th}^2} \]

For typical values \((W/L) = 10, I_D = 100 \mu\text{A}, \quad \mu_n C_{ox} = 50 \mu\text{AV}^{-2}\) we find that

\[ g_m = 320 \mu\text{AV}^{-1} = 0.32 \text{ mS} \]
How do we make a circuit which expresses $i_d = g_m v_{gs}$? Since the current is not across its "controlling" voltage, we need a voltage-controlled current source:

**Output Conductance/Resistance**

We can also find the change in drain current due to an increment in the drain-source voltage:

$$g_o = \left. \frac{\partial i_D}{\partial v_{DS}} \right|_Q = \mu_n C_{ox} \left( \frac{W}{2L} \right) (V_{GS} - V_{Tn})^2 \lambda_n \equiv \lambda_n I_D$$

The output resistance is the inverse of the output conductance

$$r_o = \frac{1}{g_o} = \frac{1}{\lambda_n I_D}$$

The (partial) small-signal circuit model with $r_o$ added looks like:

\[
\begin{align*}
    i_d &= g_m v_{gs} + \left( \frac{1}{r_o} \right) v_{ds} \\
    \text{gate} &\quad + \quad \bigcirc \quad \text{drain} \\
    v_{gs} &\quad \text{source} \\
\end{align*}
\]
MOSFET Capacitances in Saturation

In saturation, the gate-source capacitance contains two terms, one due to the channel charge's dependence on $V_{GS} \left( \frac{2}{3}WLC_{ox} \right)$ and one due to the overlap of gate and source ($WC_{ov}$ where $C_{ov}$ is the overlap capacitance in fF per µm of gate width)

$$C_{gs} = \frac{2}{3}WLC_{ox} + WC_{ov}$$

In addition, there is the small but very important gate-drain capacitance (just the overlap capacitance $C_{gd} = C_{ov}$).

There are depletion capacitances between the drain and bulk ($C_{db}$) and between source and bulk ($C_{sb}$). Finally, the extension of the gate over the field oxide leads to a small gate-bulk capacitance $C_{gb}$.

Complete Small-Signal Model

- All these capacitances are “patched” onto the small-signal circuit schematic containing $g_m$ and $r_o$, $g_{mb}$ is open-circuited for EECS 105 since $V_{BS} = 0$ V.
p-channel MOSFETs

- Structure is complementary to the n-channel MOSFET
- In a CMOS technology, one or the other type of MOSFET is built into a well -- a deep diffused region -- so that there are electrically isolated “bulk” regions in the same substrate

\[ n^+ \text{source} \quad p^+ \text{drain} \quad p^+ \text{source} \quad n^+ \]

\[ \text{p-type substrate} \]

p-channel MOSFET Models

- DC drain current in the three operating regions: \(-I_D > 0\)

\[ -I_D = 0 \quad A \]

\[ -I_D = \mu_p C_{ox}(W/L)(V_{SD} + V_{TH} - (V_{DD}/2))(1 + \lambda_p V_{DD}) - \lambda \mu_p V_{DD}^2 \] \( V_{DD} \leq -V_T \)

\[ -I_D = \mu_p C_{ox}(W/2L)(V_{SD} + V_{TH} + \lambda V_{DD})(1 + \lambda_p V_{DD}) \] \( V_{DD} > -V_T \)

- The threshold voltage with backgate effect is given by:

\[ V_{THp} = V_{T0p} - \gamma_p \left( \sqrt{V_{SB} - \frac{2\phi_n}{q}} - \frac{\phi_n}{q} \right) \]

Numerical values:

\( \mu_p C_{ox} \) is a measured parameter. Typical value: \( \mu_p C_{ox} = 25 \mu A/V^2 \)

\[ \lambda_p = \frac{0.1 \mu mV^{-1}}{L} \]

\( V_{TP} = -0.7 \) to \(-1.0 \) V, which should be approximately \(-V_{TH} \) for a well-controlled CMOS process
p-channel MOSFET small-signal model

- the source is the highest potential and is located at the top of the schematic