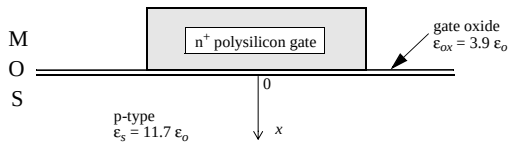
The MOS Capacitor



Oxide = SiO_2 ... a near-perfect insulator. We assume zero charge in the oxide for this course --> electric field is constant and potential is linear in the oxide.

n^+ polysilicon has a potential which is the maximum possible in silicon:

$$\phi_{n+} = 550 \text{ mV}$$

p-type substrate has potential which is $\phi_p = -60 \text{ mV} \log (N_a / 10^{10})$

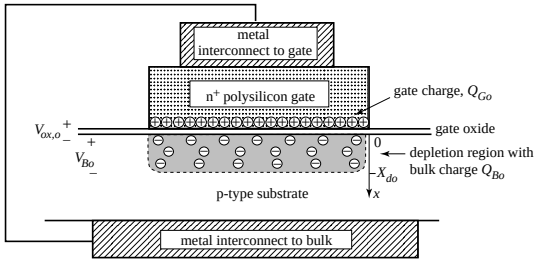
- Strategy: same as pn junction electrostatics

  first thermal equilibrium, then

  with an applied bias voltage

Qualitative Charge Distribution in Thermal Equilibrium

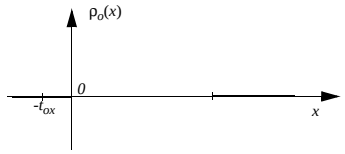
- Where to start: potential in n^+ polysilicon is known; potential in p-type substrate is known, too ... need + charge on gate, - charge in substrate --> since the silicon is p-type, this means that a depletion region forms under the gate



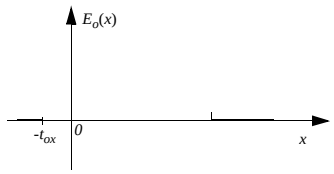
Thermal Equilibrium MOS Electrostatics

- Sketch charge density, electric field, and potential in equilibrium

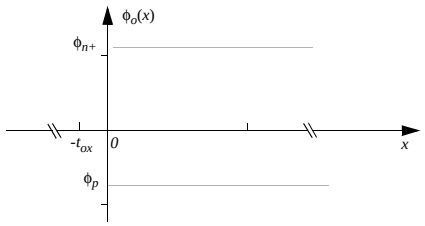
charge density



electric field



potential

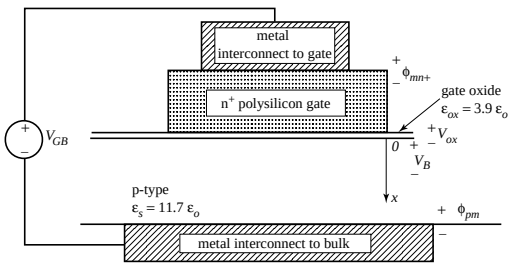


MOS Capacitor under Applied Bias

- Oxide doesn't permit any steady-state current between the n^+ poly gate and the substrate. Therefore, if we wait long enough for transient currents to die out, the electron and hole currents are zero --

$$J_n = 0 \quad \text{and} \quad J_p = 0$$

- Even though the structure isn't in equilibrium, the absence of current implies that we can relate potential to carrier concentration in the silicon substrate (since that's all we assumed in deriving the 60 mV rule.)

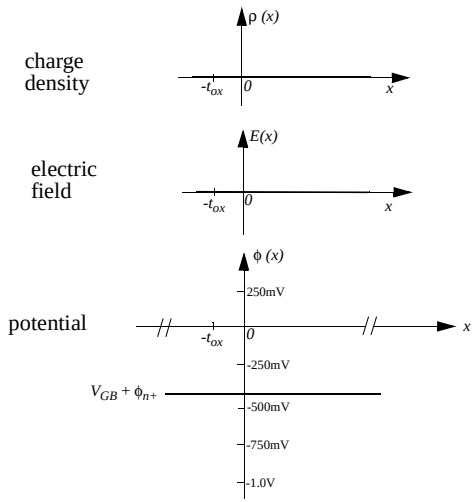


- Flatband condition: cancel built-in drop by applying the *flatband voltage*

$$V_{GB} = -(\phi_{n+} - \phi_p) = V_{FB} = -970 \text{ mV for } N_a = 10^{17}\ \text{cm}^{-3}$$

MOS Electrostatics in Flatband

- When $V_{GB} = V_{FB}$, the gate is shifted from its thermal equilibrium potential (ϕ_{n+}) to a new value of $V_{FB} + \phi_{n+} = -(\phi_{n+} - \phi_p) + \phi_{n+} = \phi_p$, which is the same potential as the p-type bulk. Therefore, there is no potential drop across the MOS structure in flatband



- If we continue to make the gate-bulk voltage more negative, the gate will take on a negative charge $Q_G < 0$. The substrate has a positive charge, which comes from holes that are attracted by the negative gate charge

MOS Capacitor in Accumulation

- Charge density, electric field, and potential in accumulation: $V_{GB} < V_{FB}$, where $V_{FB} = -0.97$ V for this example.