IC Fabrication Technology

- History:

  1958-59: J. Kilby, Texas Instruments and R. Noyce, Fairchild
  1959-70: Explosive growth in US (bipolar ICs)
  1970-85: MOS ICs introduced, RAMs, microprocessors, Japan catches up to US in volume
  1985-97: PC revolution, improved design software for complex CMOS integrated systems, US leads in microprocessors, Japan in DRAMs
  1997-2000 > 10^8 devices/chip (= 1000 Mbit dRAM), US remains competitive -- even dominates -- sectors of the market; spin-offs from IC technology in MEMS (micro electromechanical systems) for sensing acceleration

- Key Idea: *batch fabrication* of electronic circuits

  An entire circuit, say 10^6 transistors and associated wiring -- can be made in and on top of a single silicon crystal by a series of process steps similar to printing.

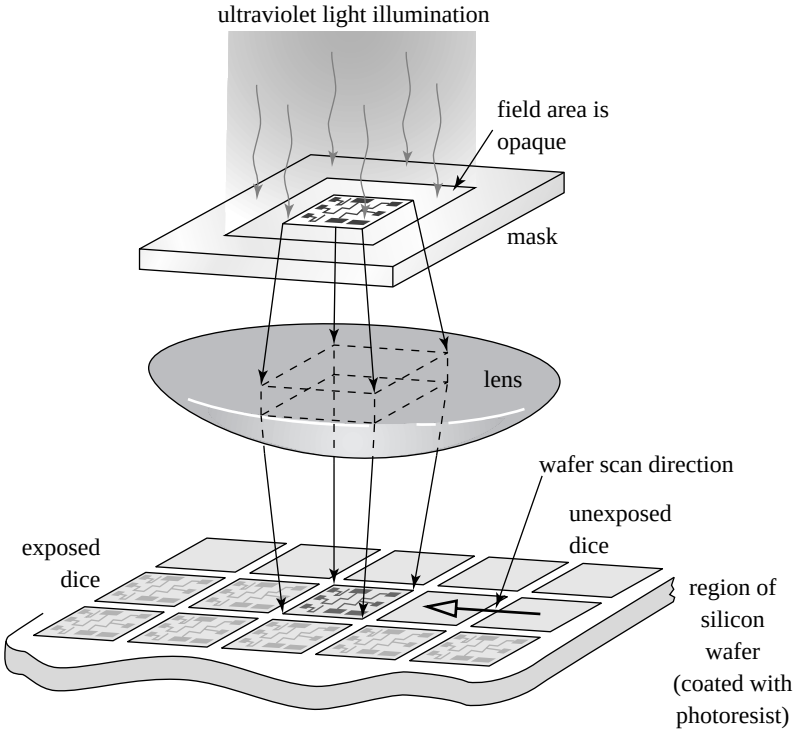
  The silicon crystal is a thin disk about the size of a small dinner plate (ca. 1997) called a *wafer*. More than 100 copies of the circuit are made at the same time.

- Results:

1. Complex systems can be fabricated reliably
2. Cost per function drops as the process improves (e.g., finer printing), since the cost per processed wafer remains about the same

Photolithography

- The essential process step: makes possible the transfer of a series of patterns onto the wafer -- all aligned to within 0.1 μm
- Process "Tool" -- *wafer stepper*



- UV-sensitive film is called *photoresist.* Regions exposed to UV dissolve in developer (for *positive* photoresist -- the type we will consider)

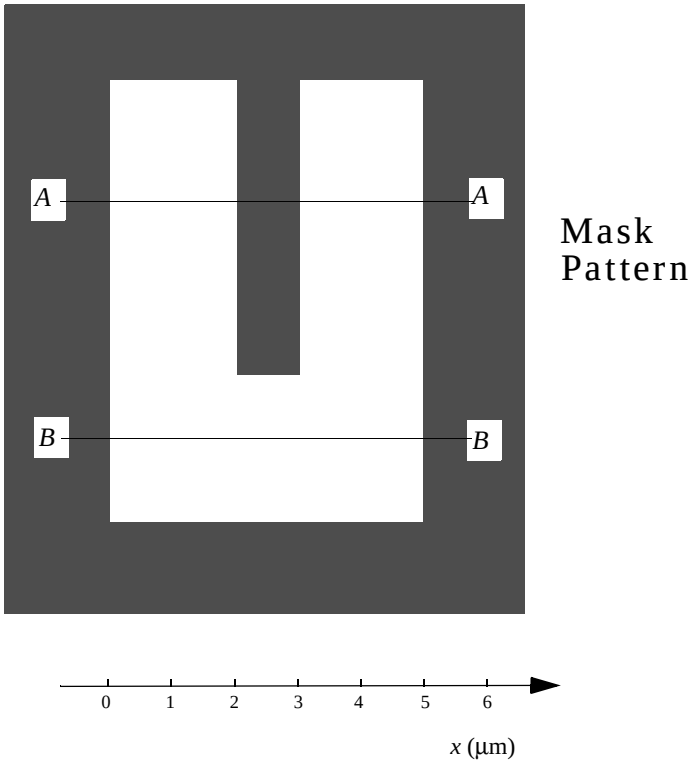
Exposure, Development, and Pattern Transfer

- Simple example of a *layout* and a *process* (or *recipe*)

  * *Layout* is the set of mask patterns for particular layers (one in this case)

  * *Process* is the sequence of fabrication steps

- Visualize by generating *cross sections* through the structure as it is built up through the process



Process Flow in Cross Sections

- Process (simplified)

  0. Clean wafer in nasty acids (HF, HNO_3, H_2SO_4, ...) --> wear gloves!

  1. Grow 500 nm of SiO_2 (by putting the wafer in a furnace with O_2

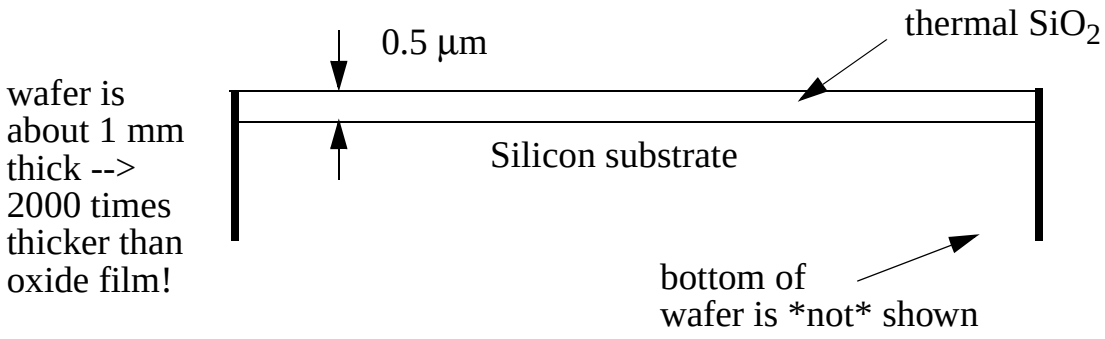
  2. Coat the wafer with 1 μm of photoresist

  3. Expose and develop the image and bake the resist to get rid solvent and to make it tougher

  4. Put wafer in a plasma etcher -- fluorine ions in plasma etch SiO_2 much faster than underlying silicon -- and etch off exposed SiO_2

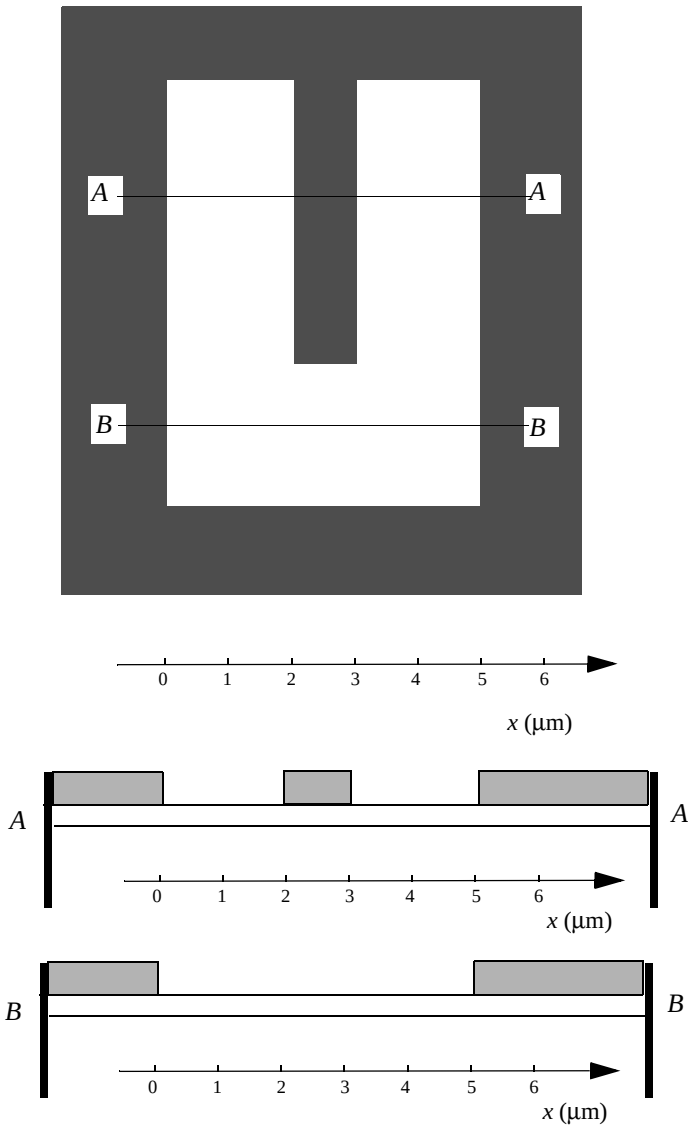
  5. Put wafer in a plasma stripper -- oxygen ions remove photoresist and leave SiO_2 untouched.

- After Step 1 (SiO_2 growth):



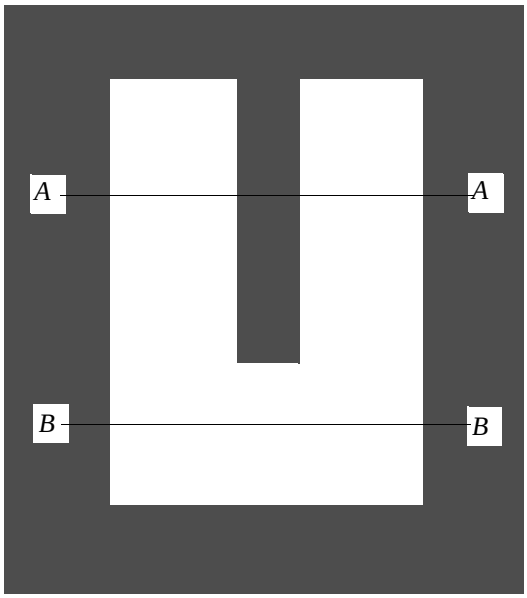
Process Flow (cont.)

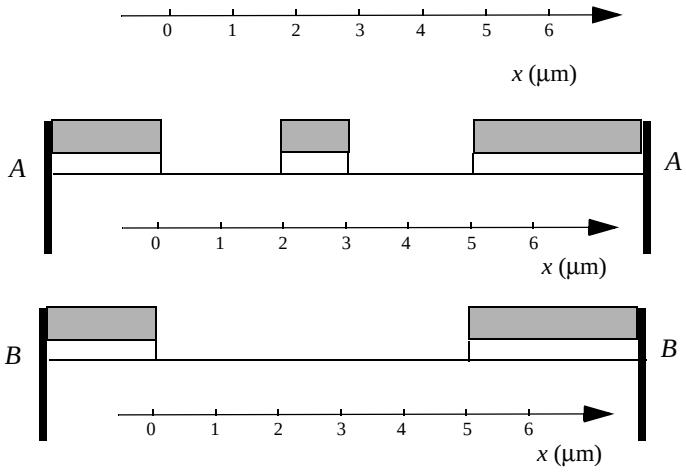
- After Step 3: photoresist has been developed from clear areas of the mask



Process Flow (cont.)

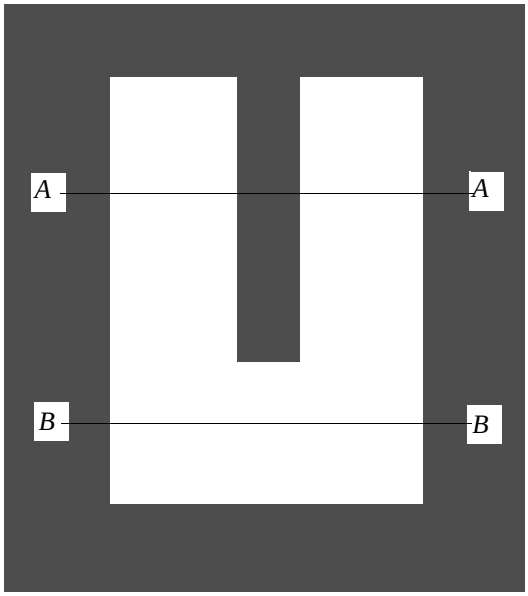
- After Step 4: oxide is etched in the fluorine plasma, without etching of the underlying silicon

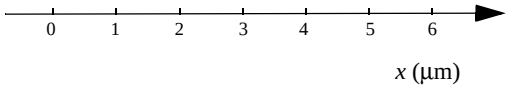


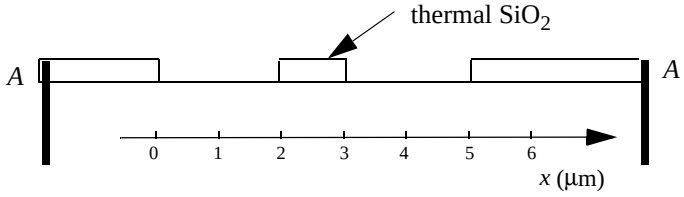


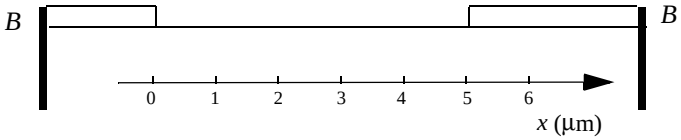
Completed Structure

- After Step 5: oxygen plasma strips (i.e., etches) the photoresist





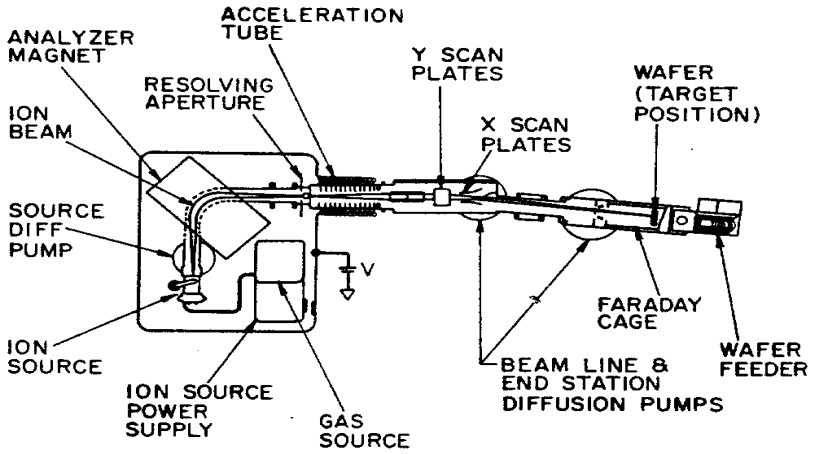




IC Fabrication Processes

- Ion Implantation

  ions are accelerated to energies of 20 keV - 3 MeV and bombard the silicon wafer in a collimated beam



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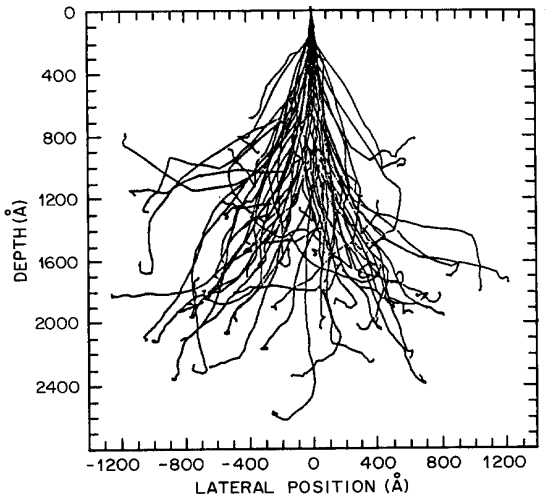
  ion tracks in the silicon crystal (simulation)



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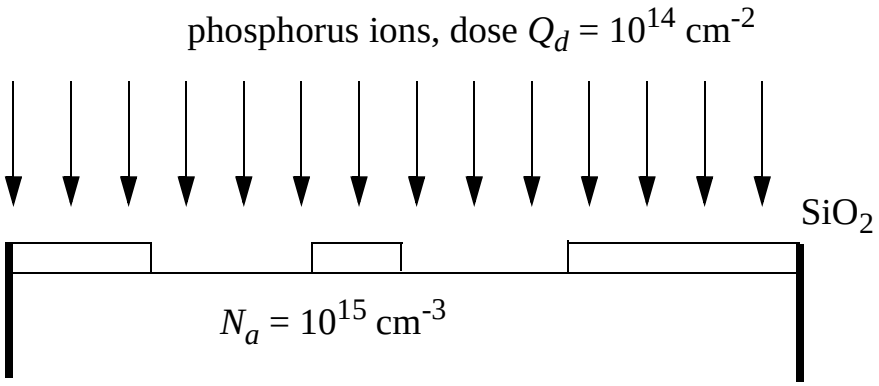
  damage from implantation can be *annealed* by heating the wafer in a furnace to $T > 900\ ^{o}C$.

Doping by Ion Implantation

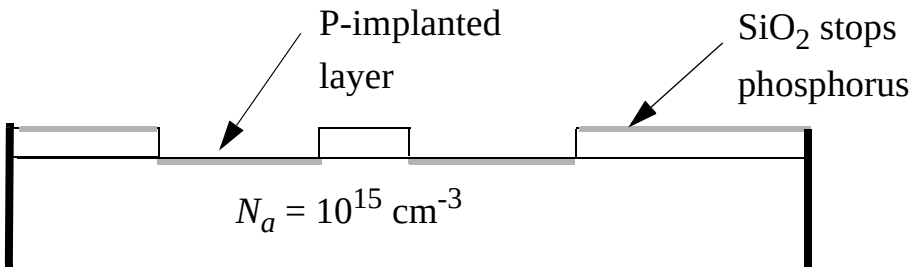
- *Dose* = ion beam flux (# cm^{-2} s^{-1}) x time for implant ... units # cm^{-2}

  Example:



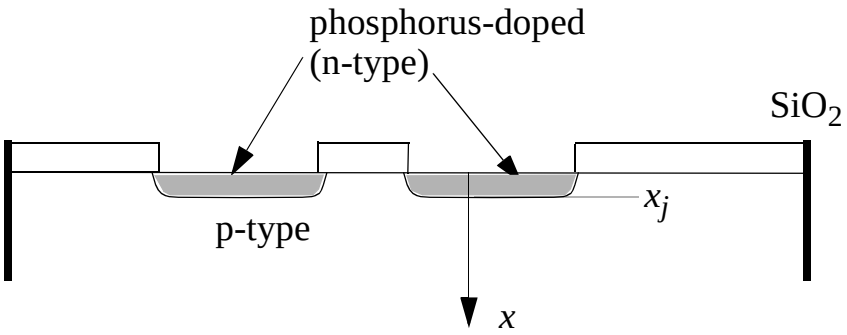
  SiO_2 film masks the implant by preventing ions from reaching the underlying silicon (assuming it's thick enough)

  > after implantation, the phosphorus ions are confined to a damaged region near the silicon surface :



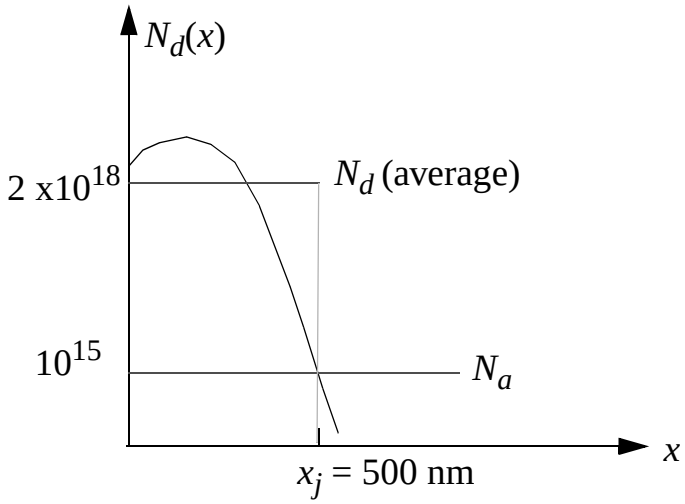
Doping by Ion Implantation (cont.)

- Annealing heals damage and also redistributes the ions (they diffuse further into the silicon crystal)



  x_j is the *junction depth* and is the point where $N_d = N_a$

- Details of $N_d(x)$ ... later in an advanced course. We will use the average concentration in the n-type region for a given junction depth here.



- Average donor concentration in n-type layer = $N_d = Q_d / x_j$

IC Materials and Processes

- *Polycrystalline silicon (polysilicon)*: silicon deposited from a gas at temperatures around 600 ^{o}C, made up of small crystallites (grains), so-so conductor when heavily doped with phosphorus, but can survive very high temperatures. Useful for making micromechanical structures

- *Deposited oxides*: silicon dioxide deposited from a gas at temperatures from 425 ^{o}C to 600 ^{o}C, boron and phosphorus are sometimes added to allow it to flow. These oxides are known as “CVD” oxides for “chemical vapor deposition.”

- *Metals*: aluminum is the standard “wire” for ICs and is usually deposited by “sputtering.” Tungsten (grown from a gas reaction) is sometimes used, with increasing interest in copper.

In order to make an IC, we need

1. the mask patterns (the *layout*)

2. the sequence of fabrication steps (the *process* ... or *recipe*)

Depicting Mask Pattern Overlays

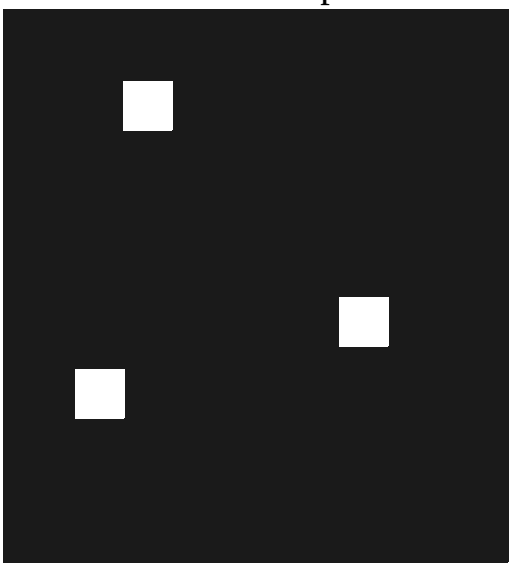
Problem: some mask plates are mostly black --> difficult to depict in the CAD layout tool since the pattern for that mask will cover underlying masks (even with high resolution color and clever "fill" patterns).

Solution: draw the negative of mostly black mask patterns in the layout editor and then label that mask carefully, so that you remember to make the inverse!

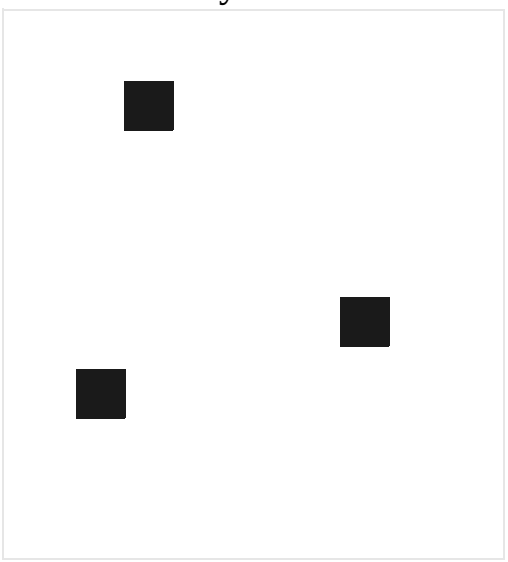
Nomenclature: "dark field" means the negative pattern is drawn
"clear field" means that the pattern is drawn

Example of a dark field mask:

actual mask plate



CAD layout of mask



label mask pattern "dark field"