*Laboratory 3:* **Configurable Amplifiers Using Small-Signal MOS Resistors**

**Preliminary Exercises**

This lab focuses on the use of MOS transistors as voltage-controlled variable resistors. In the lab, we will specifically demonstrate a gain-controllable (i.e., configurable) inverting amplifier and a bandwidth-controllable lowpass filter using op amps, resistors, capacitors, and a discrete MOS transistor.

The preliminary exercises in this section aim to prepare you for this lab. In completing these exercises, you should assume an NMOS transistor with the following parameters:

| | |
|---|---|
| Transconductance Parameter, $K_n=\mu_n C_{ox}(W/L)$: | 471 μA/V$^2$ |
| Nominal Threshold Voltage, $V_{to}$: | 1.4 V |
| Surface Potential, $2\phi_f$: | 0.66V |
| Body Effect Parameter, γ: | 0.49V$^{1/2}$ |

Other device parameters can be found in the 'cd4007ub.mod' file online, which is a SPICE model.

## 1. Gain-Controllable Amplifier

(a) For the MOS transistor circuit shown in Fig. PL3.1(a) below, calculate and tabulate (using the *Results Sheet for Preliminary Exercises*) the values of the small-signal resistance $R_{MOS}$ from drain to source for values of control voltage $V_C$ ranging from 0V to 10V, in steps of 1V. Then, plot your values of $R_{MOS}$ versus $V_C$ on a graph. Again, assume the MOS device parameters given at the beginning of this pre-lab.
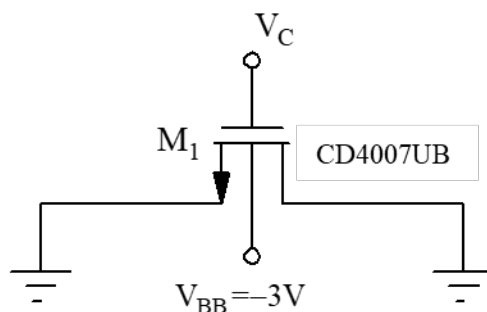


Figure PL3.1(a)

(b) For the inverting amplifier circuit shown in Fig. PL3.1(b) (which uses an op amp defined by 'lm741.mod' and an MOS transistor with parameters as in the beginning of this pre-lab defined by 'cd4007ub.mod'), calculate and tabulate (using the *Results Sheet for Preliminary Exercises*) the gain $V_o/V_i$ of this amplifier for values of control voltage $V_C$ ranging from 0V to 10V, in steps of 1V. Then, plot the gain versus $V_C$ on a graph. [<u>Hint</u>: Be careful when determining gain at $V_C=0$V.]

Assume for this pre-lab that the MOS transistors have zero leakage currents.

Figure PL3.1(b)
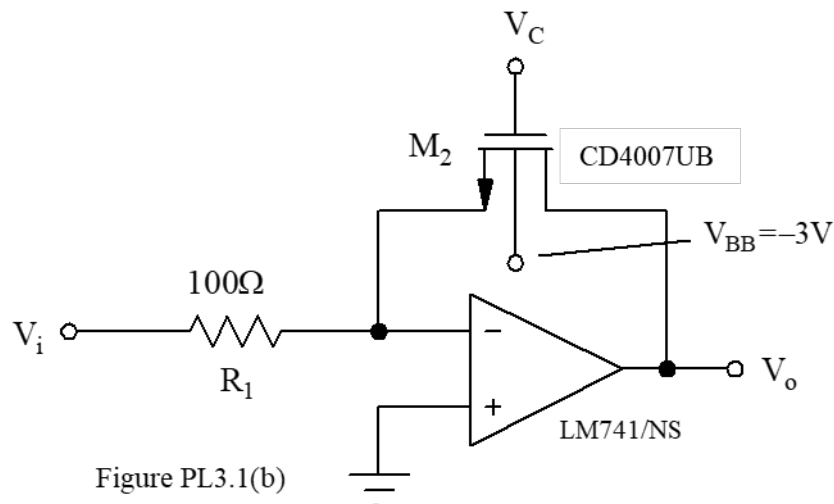
(c) Calculate and tabulate (using the *Results Sheet for Preliminary Exercises*) the 3dB bandwidth of the amplifier for values of $V_C$ ranging from 2V to 10V, in steps of 1V. Use SPICE to generate Bode plots for this amplifier, for values of $V_C$ ranging from 1V to 10V. (Plot all curves on the same graph.)

2. **Bandwidth-Controlled (Unity-Gain) Filter**

   (a) For the filter circuit shown in Fig. PL3.2(a), the op amp uses the model given in 'lm741.mod', and the MOS transistors $M_1$ and $M_2$ use the model given at the beginning of this pre-lab and in 'cd4007ub.mod'. Assuming for now that $M_1$ and $M_2$ are identical, calculate and tabulate (using the *Results Sheet for Preliminary Exercises*) the 3dB bandwidth of the filter for values of control voltage $V_C$ from 2V to 10V, in steps of 1V.

   (b) Using SPICE, generate Bode plots (all on the same graph) for the circuit of Fig. PL3.2(a) for values of $V_C$ from 2V to 10V, in steps of 1V. Use the SPICE model 'cd4007ub.mod' for each NMOS transistor and use the model in 'lm741.mod' for the op amp.

   (c) Suppose that due to fabrication mismatches, the channel length of $M_1$ was 10% larger than that of $M_2$ (everything else identical). What then is the passband gain of this filter?

   (d) Suppose that due to fabrication mismatches, the threshold voltage $V_{t1}$ of $M_1$ was 20% larger than that of $M_2$ (everything else identical). Calculate and tabulate (using the *Results Sheet for Preliminary Exercises*) the gain $V_o/V_i$ of the filter for control voltage $V_C$ values from 2V to 10V, in steps of 1V. Plot the gain $V_o/V_i$ versus $V_C$ on a graph.
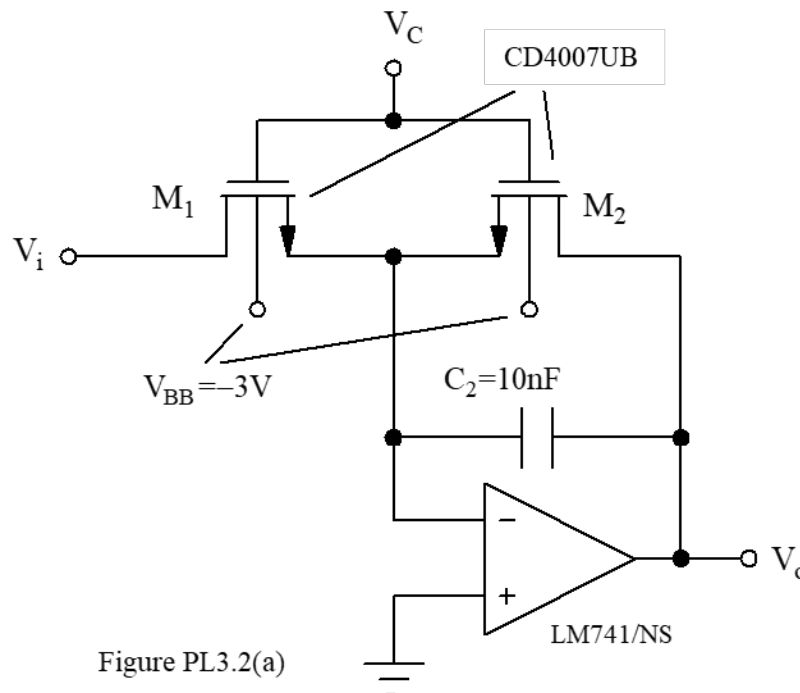
Figure PL3.2(a)

## Helpful Hints for SPICE Simulation

Some notes on creating a MOSFET instance for this lab:

(1)     For the NMOS transistor, you should use the model file on the course website, 'cd4007.mod'.

(2)     To use an NMOS transistor in your netlist, you must first include the model file using a .include statement:

```
.include <path_to_model_file>
```

(3)     Then, to create an instance of the MOSFET use the following code:

```
M<name> <drain> <gate> <source> <model_name> (W=<value> L=<value>)
```

Replace <name> with the desired name of your NMOS instance and <model_name> with the name of the NMOS model, which is defined within 'cd4007.mod'. For the CD4007UB the W is 42 µm and L is 10 µm.

(4)     To run a nested DC sweep (i.e., to sweep two sources in the same simulation), the syntax is very similar to the standard DC sweep:

```
.dc <source1> <start1> <stop1> <step1> <source2> <start2> <stop2> <step2>
```

Note that in this analysis, <source1> is swept and <source2> is stepped.

*Laboratory 3:* **Configurable Amplifiers Using Small-Signal MOS Resistors**

**Results Sheet for Preliminary Exercises**

**1. Gain-Controllable Amplifier**

Table PLR3.1. Gain-Controllable Amplifier Characteristics

| $V_C$ [V] | (a) $R_{MOS}$ | (b) Gain, $V_o/V_i$ | (c) 3dB Bandwidth |
|---|---|---|---|
| 0 | | | |
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |
| 5 | | | |
| 6 | | | |
| 7 | | | |
| 8 | | | |
| 9 | | | |
| 10 | | | |

Attach the necessary annotated plots for parts (a), (b), and (c).

## 2.  Bandwidth-Controlled (Unity-Gain) Filter

Table PLR3.2. Bandwidth-Controllable Amplifier Characteristics

| $V_C$ [V] | (a) 3dB Bandwidth | (d) Gain,  $V_o/V_i$ |
|---|---|---|
| 2 | | |
| 3 | | |
| 4 | | |
| 5 | | |
| 6 | | |
| 7 | | |
| 8 | | |
| 9 | | |
| 10 | | |

(a) Fill in the table above.

(b) Attach annotated SPICE plot.

(c) Gain, $V_o/V_i$ =  _____

(d) Fill in the table above and attach the necessary annotated plot.

## *Laboratory 3:* **Configurable Amplifiers Using Small-Signal MOS Resistors**

## **Laboratory Exercises**

### INTRODUCTION

### Objectives

This lab attempts to illustrate the small-signal operation of a nonlinear device by demonstrating a gain-controllable inverting amplifier and bandwidth-controllable lowpass filter using a small-signal MOS resistor.

### Summary of Procedures

(i) Using the HP 4155B, take sufficient data to determine the parameters needed to predict the small-signal resistance of two discrete MOS transistors under various gate bias voltages.

(ii) Build a gain-controllable inverting amplifier using an op amp, a resistor, and one of the discrete MOS transistors measured in (i).

(iii) Measure the gain and bandwidth of the gain-controllable amplifier under various MOS resistor gate bias voltages.

### Materials Required

- HP 4155B Semiconductor Parameter Analyzer
- Proto-board
- Power Supplies
- DMM
- Assorted Resistors
- CD4007UB Transistor DIP

### PROCEDURE

### 1. Characterizing MOS Transistors

[*Note*: *This part need not be done first. If an HP 4155B is not available initially, e.g., due to some of them being down or inoperable, you can do the other parts in the lab first, then characterize the NMOS transistors you used as the last step*.]

In this part of the lab, you will again use the HP 4155B Semiconductor Parameter Analyzer, this time to measure the *IV*-characteristics of two NMOS transistors contained within the CD4007UB DIP packages. For your reference, the data sheet (including the pin-out) for the CD4007UB transistor DIP is online. Note that this chip contains both NMOS and PMOS

transistors, as well as an inverter circuit. Be careful to choose two *NMOS transistors*, not PMOS, for this part.

(a) You will need to configure the HP 4155A/B/C for MOS $I_D$ versus $V_{DS}/V_{GS}$ curve measurement. Basically, you will set up the sweeps using the same procedures as in Lab 2, though this time you will configure the HP 4155B to test an NMOS device hooked up through the HP16058 Test Fixture as summarized in Table L3.1(a).

TABLE L3.1(a). HP 4155B Connections for MOS Device Curve Measurement

| HP 4155B Connector | Represented Voltage | Connect To: |
|:---:|:---:|:---:|
| SMU1 | $V_S$ | source |
| SMU2 | $V_{DS}$ | drain |
| SMU3 | $V_{GS}$ | gate |
| SMU4 | $V_B$ | bulk |

Using the hookup indicated in Table L3.1(a), use the following procedure to measure the $I_D$ versus $V_{DS}/V_{GS}$ curves (for $V_{DS}$ ranging from 0V to 5V, and $V_{GS}$ ranging from 0V to 10V, in steps of 1V, with $V_B= -3V$) and obtain a data plot for one of the NMOS transistors in your CD4007UB chip:

[The HP 4155A/B/C has two types of keys: "hard" keys, which are dedicated buttons on the front panel, and a column of "soft" keys, just to the right of the screen. In the procedure below, a $\boxed{\text{KEY}}$ is a hard key, and a $\boxed{\text{KEY}}$ is a soft key.]

(1) $\boxed{\text{CHAN}}$ to navigate to the "CHANNEL DEFINITION" screen. Name the channels according to Table L3.1(a) above. Be sure to set $V_{DS}$ to VAR1 and $V_{GS}$ to VAR2, which will allow you to sweep $V_{DS}$ while stepping $V_{GS}$.

(2) $\boxed{\text{MEAS}}$ to get to the "SWEEP SETUP" screen. Set the sweep parameters so that $V_{DS}$ is swept from 0V to 5V (in steps of at most 100mV) and $V_{GS}$ is swept from 0V to 10V in 1V steps. Be sure to ground $V_S$ and set $V_B$ to -3V.

(3) $\boxed{\text{DISPLAY}}$ to get to the "DISPLAY SETUP" screen. Here you should set the axes according to the type of characteristic you want to plot. For example, $I_d - V_{DS}$ curves would be plotted with $V_{DS}$ on the $x$-axis and $I_D$ on the $y$-axis. Note that for the $I_D - V_{GS}$ curves, you should set $V_{DS}$ to be a CONST voltage while sweeping $V_{GS}$.

(4) $\boxed{\text{GRAPH/LIST}}$ to get the "GRAPHICS PLOT" window.

(5) $\boxed{\text{SINGLE}}$ to perform the measurement.

(6) SCALING , AUTOSCALING  if necessary to view the whole plot.

Now, measure the slope in the linear region of the $V_{GS}$=5V curve using a measurement line as follows:

(7) MARKER/ CURSOR  MARKER OFF  to turn marker on (the soft key should now read MARKER ON ); move it to first point with the        knob.

(8) MARKER SKIP  to move from curve to curve in the characteristic until you reach the $V_{GS}$=5V curve.

(9) CURSOR OFF  one time to turn on the short cursor. The soft key should now read CURSOR SHORT.

(10) LINE , CURSOR TO MARKER  to move the currently selected cursor to the current marker position.

(11) LINE , LINE SELECT NONE  to turn line options on (the soft key should now read LINE SELECT 1 ).

(12) SELECT CURSOR 1  to switch the currently selected cursor to CURSOR 2. The soft key should now read SELECT CURSOR 2 .

(13) Move the marker to the second point with the ⊙ knob, then press CURSOR TO MARKER  to move the currently selected cursor (CURSOR 2) to the new marker position.

(14) ⎡LINE⎤
    ⎣ OFF ⎦ to turn on the line, which should be drawn between the two cursors you
    have positioned. The soft key should now read ⎡LINE⎤
                                                  ⎣ ON ⎦.

(15)   You can then now read the intercept and gradient values for the drawn line from
    the display. Be sure that grad mode is off.

From the slope just determined, calculate the value of $r_{ds}$ in the linear region for this
transistor with $V_{GS}$=5V.

(b) With the same transistor-to-test fixture hookup as in (a), measure the $I_D$ versus $V_{GS}$
characteristic for values of $V_B$ ranging from 0 to −5V in 1V increments (with $V_{DS}$ =
50mV), plot it, and determine the zero-bulk-bias threshold voltage for your NMOS
device using the following procedure:

(1) ⎡GRAPH/LIST⎤ to get the "GRAPHICS PLOT" window.

(2) ⎡SINGLE⎤ to perform the measurement.

(3) ⎡SCALING⎤ , ⎡AUTOSCALING⎤ if necessary to view the whole plot.

Now, determine the threshold voltage by locating the apparent point where the curve
intersects the $V_{GS}$-axis (c.f., Fig. L3.1 ). Do this using the measurement line as described
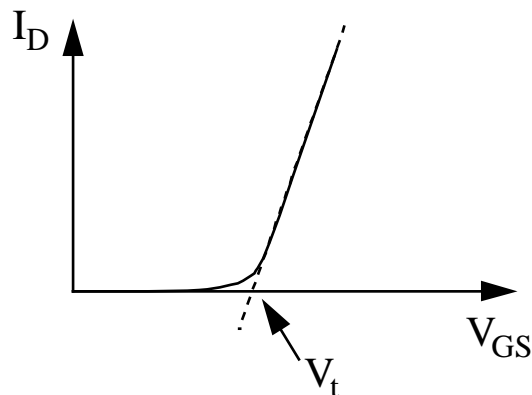in part (a), being sure to place the measurement line along the steep part of the curve.



Figure L3.1      Determination of  $V_t$ from the
$I_D$ vs.  $V_{GS}$ curve for a linear
MOSFET.

(c) Still with the same transistor-to-test-fixture hookups, measure the drain-to-source
resistance $r_{ds}$ (on a log scale) versus $V_{GS}$ characteristic as follows:

(1) $\boxed{\text{DISPLAY}}$ to get to the "DISPLAY SETUP" page. This page defines the plot(s) to be measured when you hit $\boxed{\text{SINGLE}}$ later on. At this point, the page is setup to plot $I_D$ (defined in the Y1-axis column) versus $V_{GS}$ (defined in the X-axis column).

(2) Move the pointer to the Y1-axis column and select "RDS" from the soft-keys as the Y1-axis name. "RDS" is a defined function (defined on the "CHANNELS: USER FUNCTION DEFINITION" page) that calculates the $r_{ds}$ resistance for you from the $I_D$ versus $V_{GS}$ data that the HP 4155B actually measures. Switch to "LOG" scale for the Y1-axis and set the minimum and maximum scale values to 0 and 100000, respectively. Now, you have effectively set up the HP 4155B to measure the MOS small-signal resistance $r_{ds}$ as a function of gate voltage $V_{GS}=V_C$.

(3) $\boxed{\text{GRAPH/LIST}}$ to get the "GRAPHICS PLOT" window.

(4) $\boxed{\text{SINGLE}}$ to perform the measurement.

(5) $\boxed{\text{SCALING}}$, $\boxed{\text{AUTOSCALING}}$ if necessary to view the whole plot.

(d) Repeat steps (a) through (c) for another MOS transistor on your CD4007UB chip. Keep track of which transistor is which. Call the first one $M_1$ and call the second one $M_2$.

## 2. Gain-Controllable Amplifier

(a) Hook up the circuit in Fig. PL3.1(b) and apply a 0.2Vpp, 10-kHz sinewave to the input of the circuit. Use your oscilloscope to measure the low frequency gain $V_o/V_i$ and 3dB bandwidth of this amplifier for values of control voltage $V_C$ ranging from 2V to 10V, in steps of 1V. Tabulate your data using the "measured" sections of Table LR3.2 in the *Results Sheet for Laboratory Exercises*, then plot the gain versus $V_C$ and 3dB bandwidth versus $V_C$ on separate graphs.

(b) [Note: You can do this part after the lab period, if necessary.] Extract values for $K_n$ and $V_{TN}$ from your part 1 measurements and use these to fill in the "calculated" portions of Table LR3.2 in the *Results Sheet for Laboratory Exercises*. Then plot the gain versus $V_C$ and 3dB bandwidth versus $V_C$ on the same graphs as your measured data, being sure to delineate which graph is which. Comment on any discrepancies between measured and calculated data.

(c) Next, set the amplitude of the input sinewave to 5Vpp and the frequency to 10kHz. Print out a plot of the ensuing output waveform. Does the waveform look strange? Why? Now what is the gain of the amplifier? (Determine gain based on peak signals, whether they are sinusoidal or not.)

## 3. Bandwidth-Controlled (Unity-Gain) Filter

(a) Hook up the circuit in Fig. PL3.2(a) and apply a 0.2Vpp, 10-kHz sinewave to the input of the circuit. Use your oscilloscope to measure the low frequency gain $V_o/V_i$ and 3dB bandwidth of this amplifier for values of control voltage $V_C$ ranging from 1V to 10V, in steps of 1V. Tabulate your data using the "measured" sections of Table LR3.3 in the

*Results Sheet for Laboratory Exercises*, then plot the gain versus $V_C$ and 3dB bandwidth versus $V_C$ on separate graphs.

(b) [Note: You can do this part after the lab period, if necessary.] Using your extracted values for $K_n$ and $V_{TN}$ from Part 2(b) above, fill in the "calculated" portions of Table LR3.3 in the *Results Sheet for Laboratory Exercises*. Then plot the gain versus $V_C$ and 3dB bandwidth versus $V_C$ on the same graphs as your measured data, being sure to delineate which graph is which. Comment on any discrepancies between measured and calculated data.

(c) Next, set the amplitude of the input sinewave to 5Vpp and the frequency to 10kHz. Print out a plot of the ensuing output waveform. Does the waveform look better or worse than the waveform seen under a large input for the circuit in Part 2? Why?

*Laboratory 3:* **Configurable Amplifiers Using Small-Signal MOS Resistors**

**Results Sheet for Laboratory Exercises**

**NAME:** _____          **LAB SECTION:** _____

1. **Characterizing MOS Transistors**

   (a) Attach annotated HP 4155B plot of $I_D$ vs. $V_{DS}/V_{GS}$ curves for both $M_1$ and $M_2$. Show all calculations on the plot.

   $r_{ds1}$(for $M_1$ with $V_{GS1}$=5V) =   _____

   $r_{ds2}$(for $M_2$ with $V_{GS2}$=5V) =   _____

   (b) Attach annotated HP 4155B plot of $I_D$ versus $V_{GS}$. Show all calculations on the plot.

   $V_{t1}$(for $M_1$) =   _____

   $V_{t2}$(for $M_2$) =   _____

   (c) Attach annotated HP 4155B plot of $r_{ds}$ versus $V_{GS}$.

2. **Gain-Controllable Amplifier**

   (a) Fill in the columns associated with the "measured" portions of Table LR3.2.

   Attach the required annotated plots.

   (b) Fill in the columns associated with the "calculated" portions of Table LR3.2.

   Plots your results as required on the same graph as the measured data.

Table LR3.2. Gain-Configurable Amplifier Characteristics

| $V_C$ [V] | Gain, $V_o/V_i$ | | 3dB BW | |
|---|---|---|---|---|
| | 2(a) Measured | 2(b) Calculated | 2(a) Measured | 2(b) Calculated |
| 2 | | | | |
| 3 | | | | |
| 4 | | | | |
| 5 | | | | |
| 6 | | | | |
| 7 | | | | |
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |

(c) Attach an annotated plot of the output waveform.

Does the waveform look strange? Why?

Gain, $V_o/V_i = $ _____

### 3. Bandwidth-Controlled (Unity-Gain) Filter

(a) Fill in the columns associated with the "measured" portions of Table LR3.3.

Attach the required annotated plots.

(b) Fill in the columns associated with the "calculated" portions of Table LR3.3.

Plots your results as required on the same graph as the measured data.

Table LR3.3. Bandwidth-Configurable Amplifier Characteristics

| $V_C$ [V] | Gain, $V_o/V_i$ | | 3dB BW | |
|---|---|---|---|---|
| | 3(a) Measured | 3(b) Calculated | 3(a) Measured | 3(b) Calculated |
| 2 | | | | |
| 3 | | | | |
| 4 | | | | |
| 5 | | | | |
| 6 | | | | |
| 7 | | | | |
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |

(c) Does the waveform look better or worse than the waveform seen under a large input for the circuit in part 2? Why?

## 4. GENERAL QUESTIONS

Using the data obtained in Part 3(a) of the laboratory exercises, determine the percent mismatch in $K_n$ and $V_t$ between these two transistors. Percent mismatch can be determined using the following formula:

$$\%\text{Mismatch} = 100 \times \frac{P_2 - P_1}{P_{avg}} = 2 \times 100 \times \frac{P_2 - P_1}{P_2 + P_1}.$$

% Mismatch in $K_n$ = _____

% Mismatch in $V_t$ = _____