EE 105 | Discussion 4

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Discussion Outline

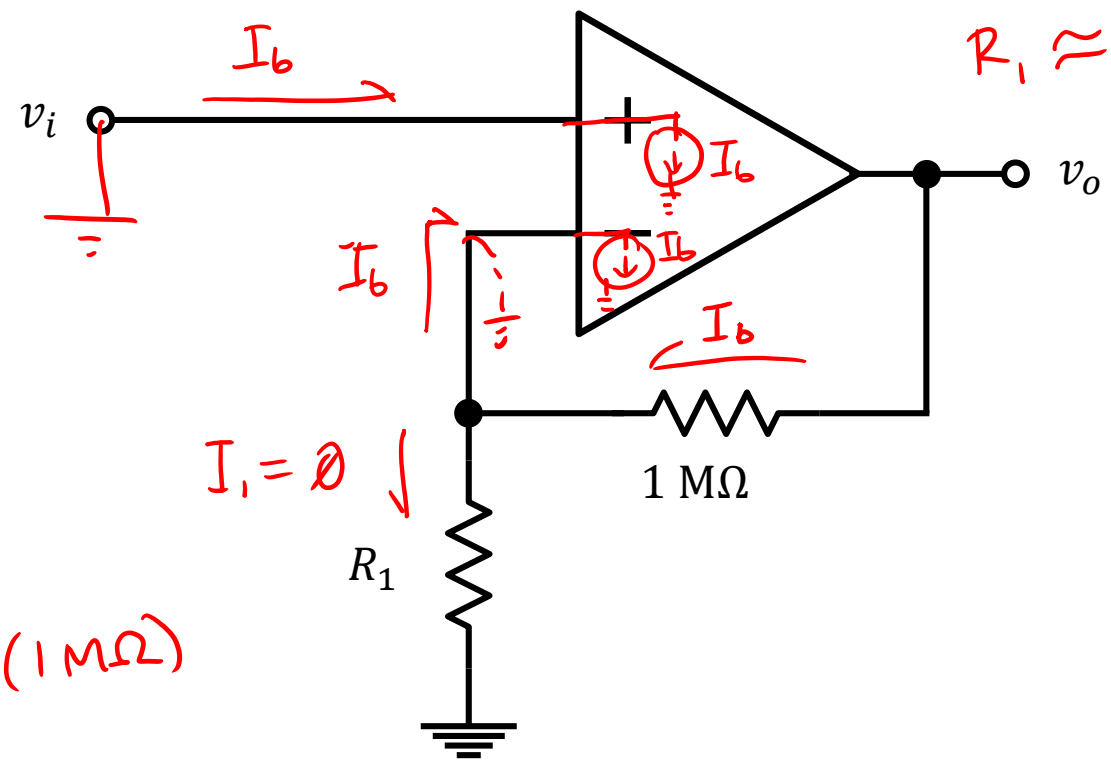
- Review offset voltage & input bias nonidealities
- Combine multiple limitations (finite bandwidth, slew rate, output saturation) into one problem
- Diode applications: review Homework 2, Question 7

Input Bias Current

- The circuit below has a closed-loop gain of 100 V/V
- Input bias current, $I_{bias} = 200\ nA$
- What's v_o when v_i is 0 V?

$A_{cl} = \left(1 + \frac{R_2}{R_1}\right) = 100\ V/V$

$R_1 \approx 10\ k\Omega$



$v_o = I_b \cdot R_2$

$= (200\ nA)(1\ M\Omega)$

$v_o = 200\ mV$

Input Offset Voltage

- Now consider an input offset voltage, $V_{OS} = \pm 2\ mV$
- What's the largest possible v_o when v_i is 0 V?

Output due only to V_{OS}

$100\ V/V$

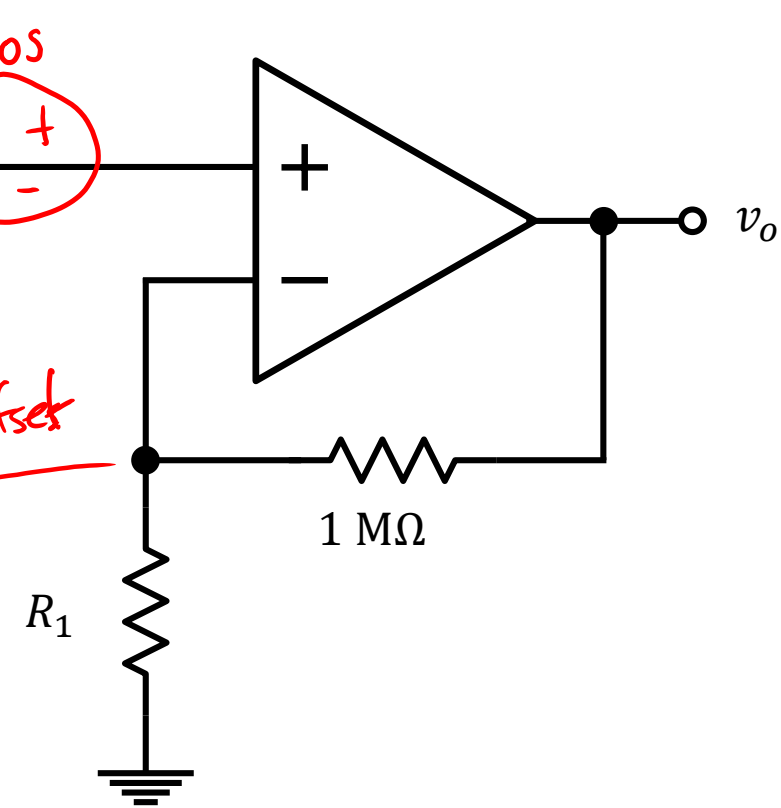
$v_o = A_{CL} v_{+-} \pm 2mV$

$= \pm 200\ mV$

Worst-case total output offset

$v_o = 200\ mV + 200\ mV$

$= 400\ mV$



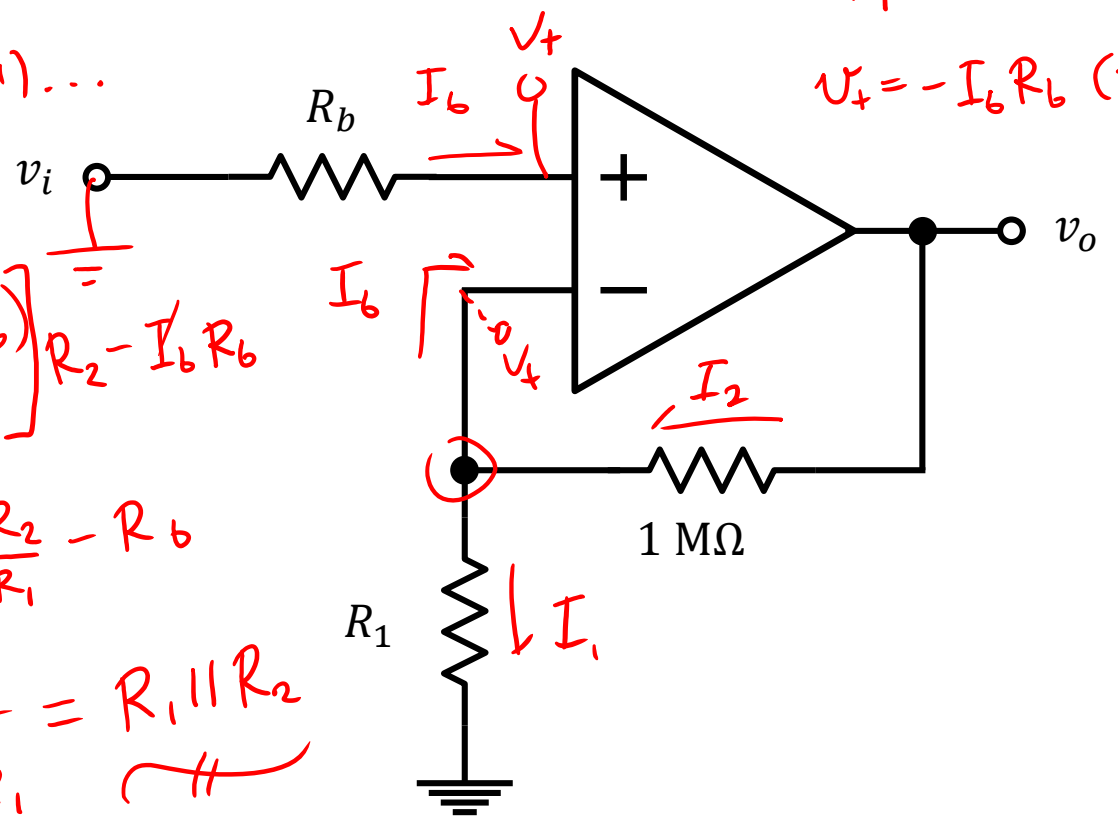
Bias-Current Compensation

- Find the value of R_b required to null the effects of I_{bias} on v_o

$v_o = I_2 R_2 + v_+ \quad (1)$ $\qquad I_2 = I_b + I_1 = I_b + \frac{v_+}{R_1} \quad (2)$

$v_+ = -I_b R_b \quad (3)$

(2) & (3) into (1)...



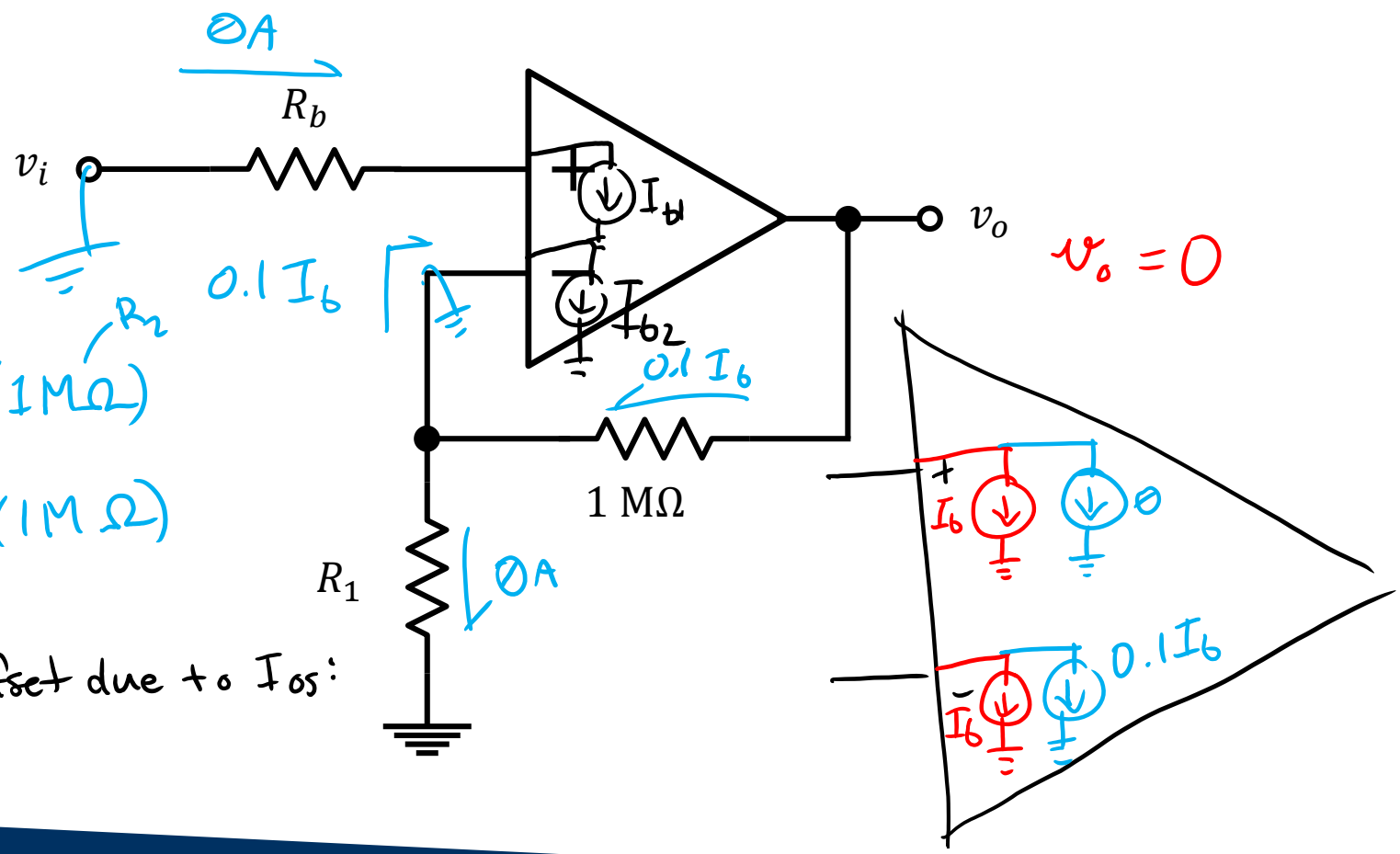
$$v_o = \left[I_b + \frac{(-I_b R_b)}{R_1}\right] R_2 - I_b R_b$$

$$0 = R_2 - R_b \frac{R_2}{R_1} - R_b$$

$$R_b = \frac{R_2}{1 + R_2/R_1} = R_1 \| R_2$$

Bias Current Offset

- If the bias current offset is 10% of I_{bias}, what's the resulting v_o (ignoring V_{OS})? $I_{b1} = I_b$ & $I_{b2} = I_b(1.1)$



$v_o = (0.1 I_b)(1 M\Omega)$

$= (20\ nA)(1 M\Omega)$

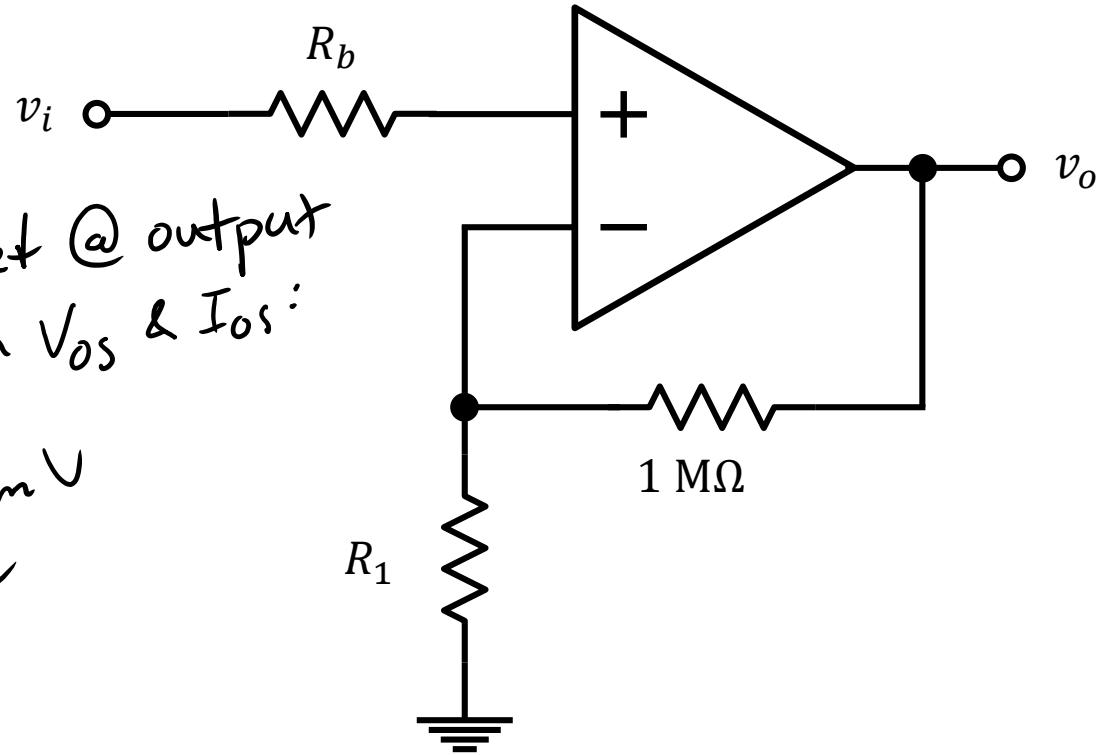
$= 20\ mV$

total output offset due to I_{os}:

$v_o = 20\ mV$

Bias Current & Voltage Offsets

- Now include V_{OS} and I_{OS} to find the worst-case dc voltage at the output in this bias-current compensated circuit



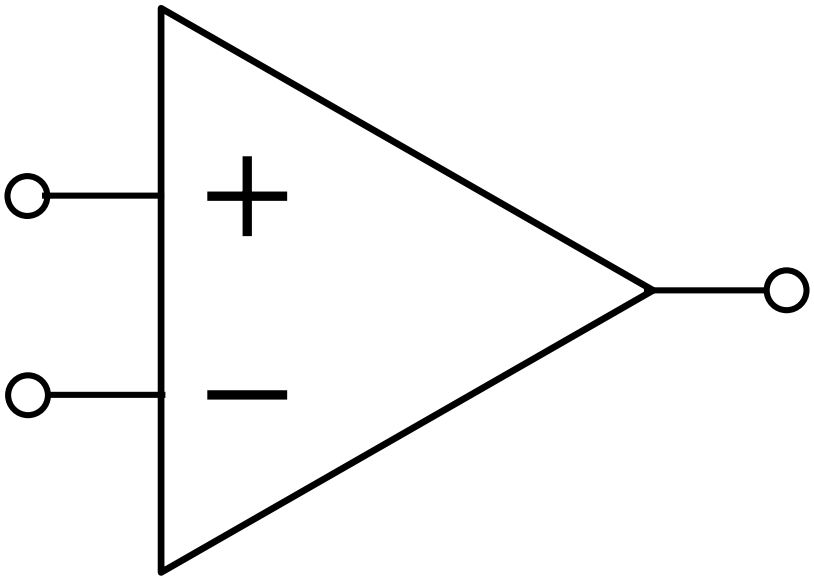
total offset @ output due to both V_{OS} & I_{OS}:

$v_o = 220\ mV$

Designing w/ Op Amps

- Let's look at how you might be constrained by a COTS (commercial off-the-shelf) part when trying to design a circuit

- $f_t = 20\ MHz$
- Slew rate, SR $= 10\,\frac{V}{\mu s}$
- Output saturation, $V_{o,max} = 10\ V$



Designing w/ Op Amps

- In noninverting configuration, if $A_{CL} = 10\frac{V}{V}$ & $V_i = 0.5\ V$ what's the maximum frequency before output distortion occurs?

- ❑ $f_t = 20\ MHz$
- ❑ $SR = 10\frac{V}{\mu s}$
- ❑ $V_{o,max} = 10\ V$

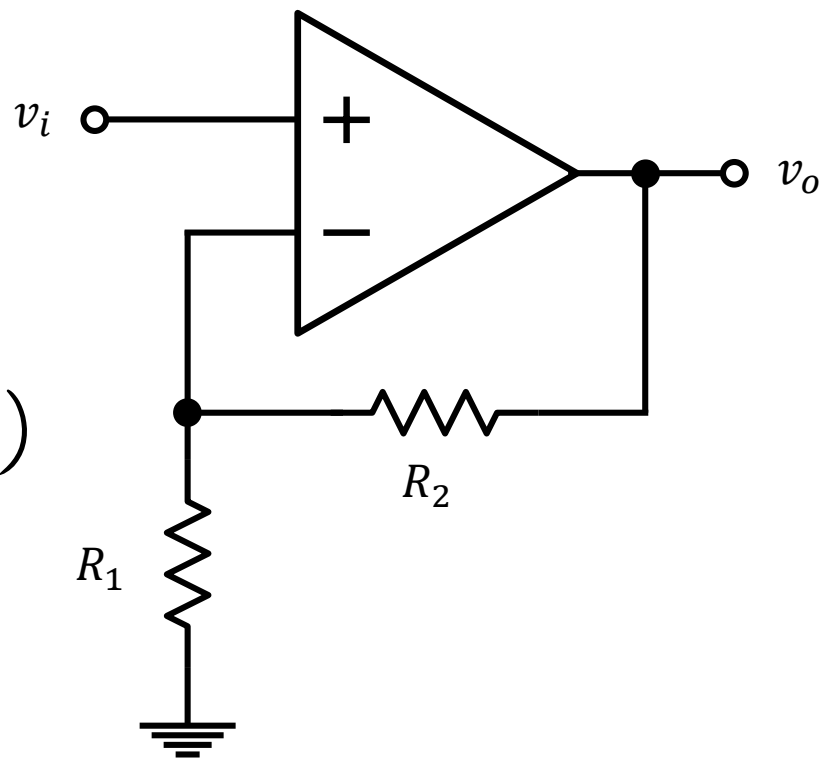
$A_{cl} V_i$

$$SR = \frac{dv_o}{dt} = \omega_{max} V_o$$

$$\frac{10V}{\mu s} = \omega_{max}\left(10\frac{V}{V}\right)(0.5V)$$

$$\omega_{max} = 2\times 10^{6}\ rad/sec$$

$$f_{max} = 318\ kHz$$



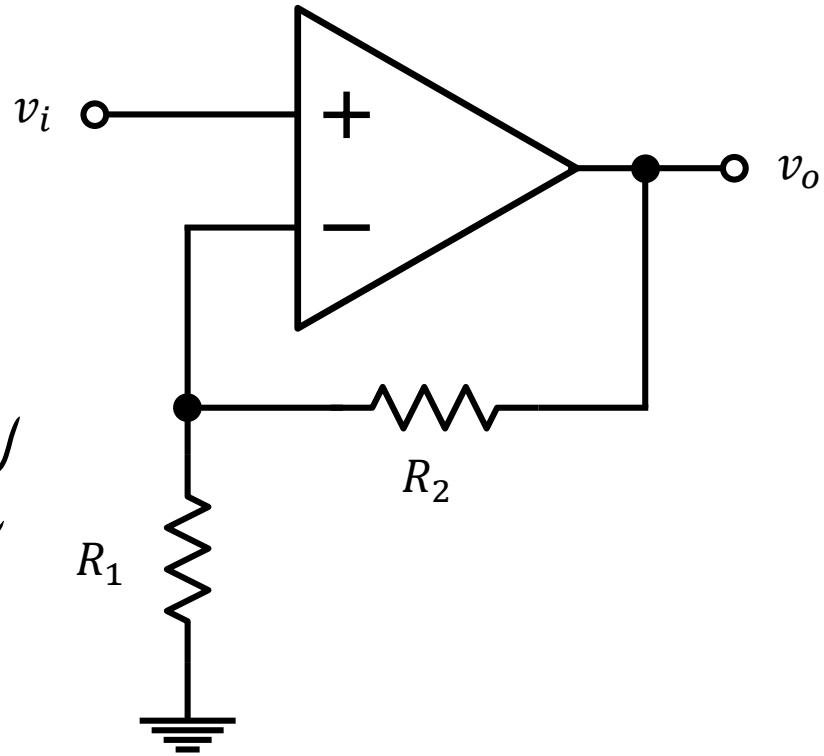
Designing w/ Op Amps

- If $f = 200\ kHz$, what's the maximum V_i before output distortion occurs?

- ❑ $f_t = 20\ MHz$
- ❑ $\mathrm{SR} = 10\,\frac{V}{\mu s}$
- ❑ $V_{o,max} = 10\ V$ V_o

$$\frac{10\,V}{\mu s} = (2\pi \cdot 200\,kHz)(10\,V_i)$$

$$V_i = \frac{10 \times 10^6}{2\pi \times 2 \times 10^5} = 796\ mV$$



Designing w/ Op Amps

- If $v_i = 50\ mV$, what's the useful frequency range of operation?

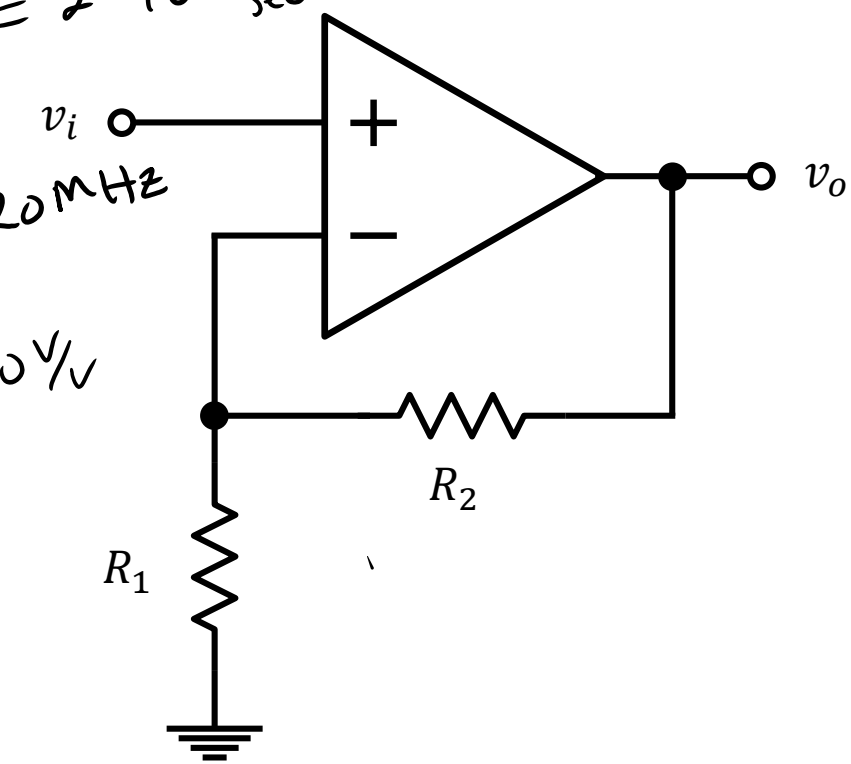
$\frac{10\ V}{\mu s} = \omega_{max}(10 \times 0.05)$

$\omega_{max} = 2 \times 10^7 \frac{rad}{sec}$ or $f_{max} = 3.18\ MHz$

- ✓ $f_t = 20\ MHz$
- ? SR $= 10 \frac{V}{\mu s}$
- $V_{o,max} = 10\ V$

$f_{3dB} = \frac{GBW}{A_{CL}} = \frac{f_t}{A_{CL}}$ ~ 20 MHz ~ 10 V/V

$f_{3dB} = 2\ MHz$



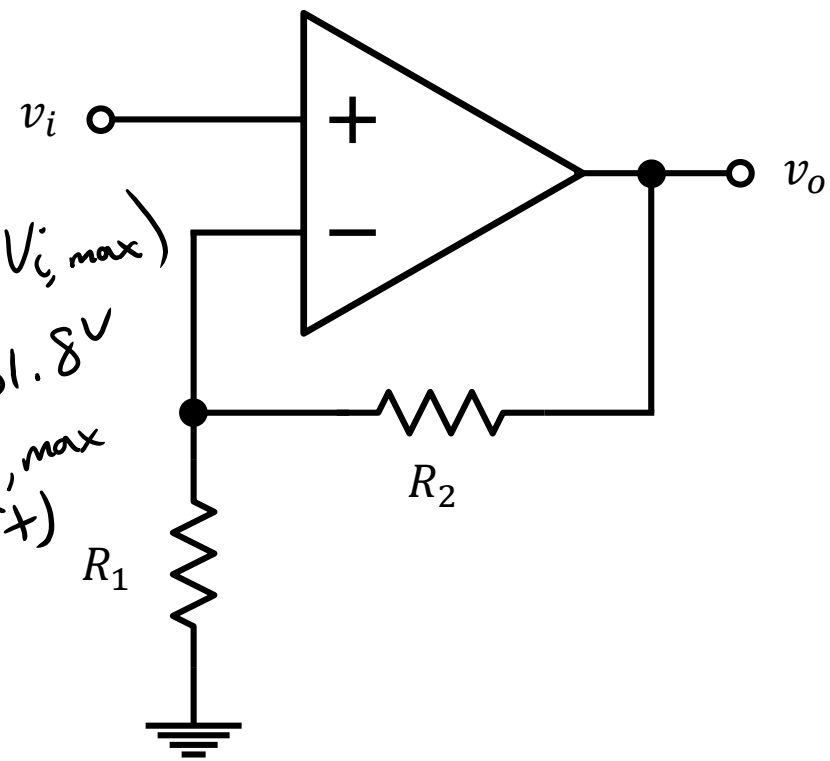
Designing w/ Op Amps

- If $f = 50\ kHz$, what's the useful range of V_i?

- ❑ $f_t = 20\ MHz$
- ? ❑ $\mathrm{SR} = 10\,\frac{V}{\mu s}$
- ✓ ❑ $V_{o,max} = 10\ V$

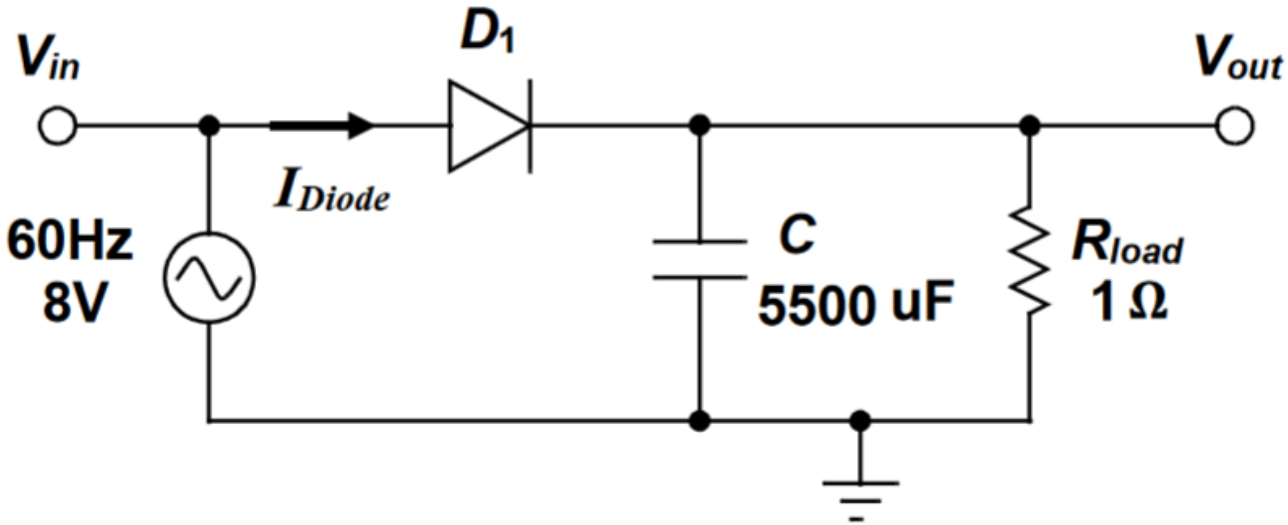
$\mathrm{SR} = \frac{10V}{\mu s} = (2\pi 50kHz)(10\ V_{i,max})$

$V_{i,max} = 3.18V \rightarrow V_o = 31.8V$ (w/o $V_{o,max}$ limit)



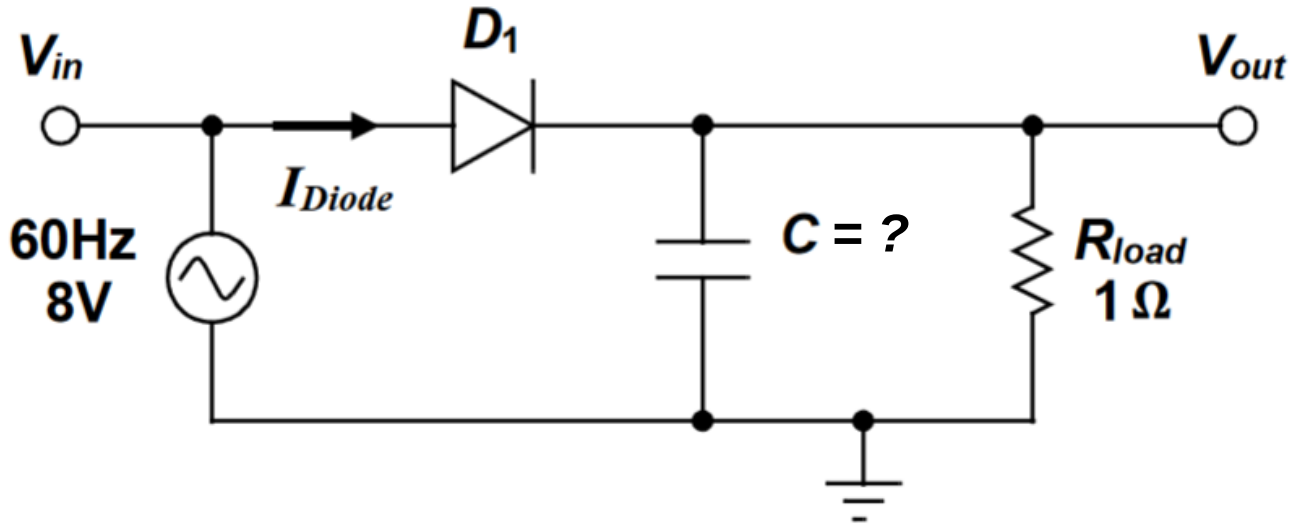
Diode Applications: Rectifiers

- What is the goal of this circuit?
  - What would the output look like with no capacitor?



Rectifier Design: $V_{ripple} = 0.5\ V$

- Simulate & iterate!



Full-Wave Rectifier

Can you think of a way to reduce ripple that doesn't require a huge capacitor?