UNIVERSITY OF CALIFORNIA
Department of Electrical Engineering and Computer Sciences

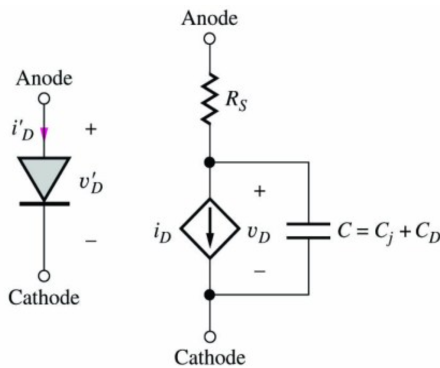
EE 105: MICROELECTRONIC DEVICES AND CIRCUITS
http://www-inst.eecs.berkeley.edu/~ee105/fa14/index.html

SPICE Model of pn Junction:
In class, we described the current-voltage and capacitance-voltage relationship as

$$i_D = I_S\left[\exp\left(\frac{qv_D}{nkT}\right)-1\right] = I_S\left[\exp\left(\frac{v_D}{nV_T}\right)-1\right]$$

$$C_j = \frac{C_{j0}A}{\sqrt{1+\frac{v_R}{\phi_j}}}$$

The parameter n is called "ideality factor". For ideal diode at normal current, n is equal to 1. In real devices, it could deviate from 1. The ideality factor can be easily extracted from the semi-log plot of i_D-vs-V_D. The SPICE model of a pn junction is shown below:



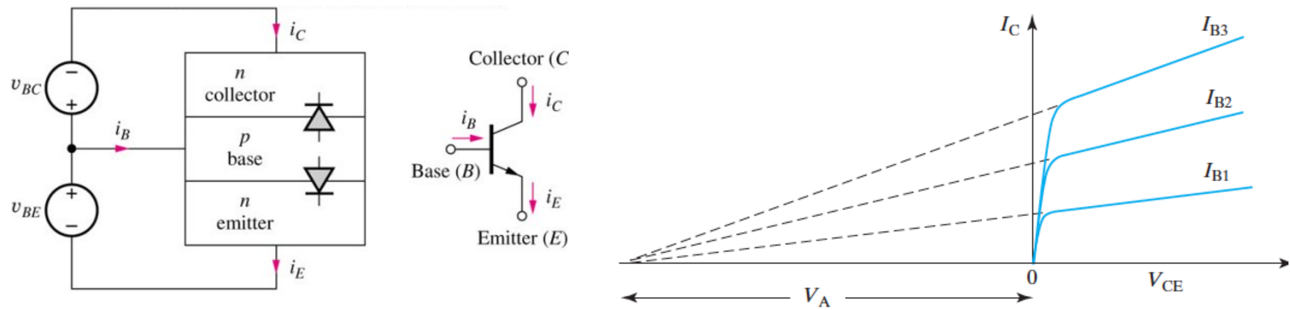
Note the expression for C_j is slightly different. If M=0.5, the expression is exactly the same as that derived in class. This corresponds to pn junctions with constant doping concentrations, i.e., N_D and N_A are constant. This is called "abrupt junction". If they are not constant, for example, in so-called "graded" pn junctions, M could deviate from 0.5.

The values of M and built-in potential, V_j (or ϕ_j), can be extracted from experimental data by curve fitting.
If M=0.5, V_j can be found by plotting

$$\frac{1}{C_j^2} \text{ vs } V_D.$$

The SPICE model also includes diffusion capacitance, C_D. It is negligible for reverse bias. We will ignore it here.
The SPICE model also includes a series resistance, R_S. Its value can be extracted from the slope of the I-V curve at high current: the total resistance at high current is dominated by R_S.

Bipolar Junction Transistor (BJT)



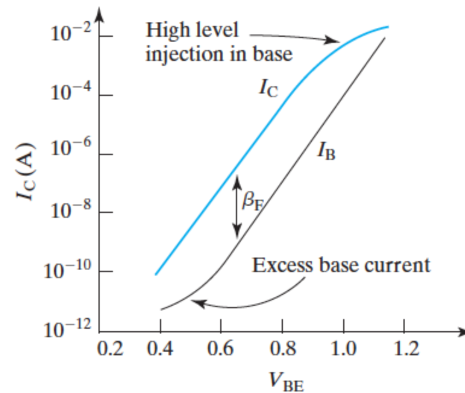
The schematic structure, symbol, and the current-voltage (I-V) characteristics of a BJT are shown above. The collector current, I_C, is controlled by base current, I_B. The flat part of the I-V curves is call “forward active” region. The flatness of the I_C curves is described by “Early voltage”, V_A:

$$r_0 \equiv \left(\frac{\partial I_C}{\partial V_{CE}}\right)^{-1} = \frac{V_A}{I_C}$$

The current gain is defined as $\beta = \dfrac{I_C}{I_B}$. The collector and the base currents are expressed as

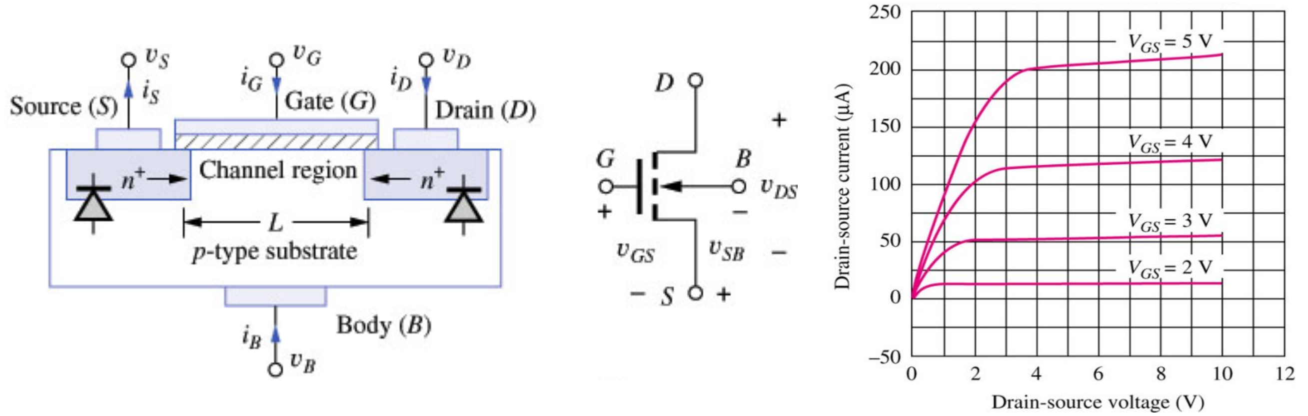
$$i_C = I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right) - \exp\left(\frac{v_{BC}}{V_T}\right)\right]$$

$$i_B = \frac{I_S}{\beta_F}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]$$



In semi-log plot of I_B and I_C vs. V_{BE}, both are linear curves except for very low and very high currents. The ratio between them is the current gain, β.

MOSFET (Metal-oxide-semiconductor field effect transistors):



The schematic structure, symbol, and current-voltage (I-V) characteristics of an N-channel MOSFET (NMOS) are shown above. The current flowing from drain to source, I_{DS}, (or electrons moving from source to drain) is controlled by the gate-source voltage, V_{GS}. On the "flat" part of the I-V curves, the so-called "saturation region", is described by the following equation:

$$i_D = \frac{\mu_n C_{ox}''}{2}\frac{W}{L}\left(v_{GS} - V_{TN}\right)^2\left(1 + \lambda v_{DS}\right)$$

$$= \frac{K_n}{2}\left(v_{GS} - V_{TN}\right)^2\left(1 + \lambda v_{DS}\right)$$

V_{TN} : threshold voltage

λ: channel length modulation parameter

The parameters can be extracted experimentally:

- Channel length modulation parameter, λ, can be extracted by measuring the slope of the I-V curves in the saturation region:

$$\lambda = \frac{1}{i_D}\frac{\Delta i_D}{\Delta v_{DS}}$$

- The threshold voltage and K_n can be found by plotting $\sqrt{i_D}$ vs. v_{GS} (ignore channel modulation here since $\lambda v_{DS} << 1$):