Announcements

- Homework 4 due next week
- Lab 2 this week
- Reading: Chapter 4
- Check out the IC seminar series, Monday 4-5pm in the Hogan Rm (531 Cory)
  - 9/26 – Rick Livengood, Intel on cool methods in chip testing and repair
Sample & Hold Function

- **Goal:** charge up load capacitor to input voltage rapidly when control voltage is switched on; hold voltage on capacitor when control is switched off
- **Applications:** analog-to-digital converters
Linear Model: $v_s$ small

- Initial condition: $v_i = 0$ V
- Gate voltage steps from 0 V to $V_{DD} = 2.5$ V

\[ i_D = \mu_n C_{ox} \left( \frac{W}{L} \right) (v_{GS} - V_{Th} - v_{DS}) \] \[ v_{GS} = V_{DD} - v_i \rightarrow \]

Gate-source voltage: $v_{GS} = V_{DD} - v_i$

Drain-source voltage: $v_{DS} = v_s - v_i$

\[ i_D \approx \left[ \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{DD} - V_{Th}) \right] (v_s - v_i) \]

Equivalent Circuit

\[ R_{DS} = \left\{ \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{DD} - V_{Th}) \right\}^{-1} \]
Example

\[ \mu_n C_{ox} = 50 \mu A/V^2, \ V_{GS} = V_{DD} = 2.5 \, V, \ V_{Tn} = 0.5 \, V, \]
\[ L = 0.6 \, \mu m \]

If we want \( R_{DS} = 100 \, \Omega \), then the MOSFET width must be:

\[ W = \frac{L}{R_{DS}\left[\mu_n C_{ox}(V_{DD} - V_{Tn})\right]} = \frac{0.6}{100 \cdot 50 \cdot 10^{-6} (2)} = 60 \, \mu m \]

For an efficient layout, this transistor with \( W/L = 100 \) should be folded ... see example in Chapter 4.

---

Example Waveform

\[ v_i(t) = v_s \left(1 - e^{-t/R_{DS}C_L}\right) \]

\[ t \]

\[ v_i(t) \]

50 mV

0.63(50) = 31.5 mV
Sampling Error

Absolute error: \( e = v_i - v_s \)

Relative error: \( \varepsilon = e / v_s \)

\[ \varepsilon = \frac{v_s - v_i}{v_s} \left(1 - e^{-t_s / R_{on}C_L}\right) \]

\( t_s \) is the sampling time (time interval where \( V_{GS} = V_{DD} \))

\[ \varepsilon = e^{-t_s / R_{on}C_L} \]

Example case: \( R_{DS} = 100 \, \Omega, C_L = 500 \, fF \rightarrow \tau = 50 \, ps \)

For 16 bit precision, we need the relative error \( \varepsilon < 2^{-16} = 1.5 \times 10^{-5} = 15 \, \text{ppm (parts per million)} \)

\[ t_s = -\tau \ln(\varepsilon) = \tau(11.1) = 554 \, ps \]

Sampling Large Voltages

If the source (a.k.a. input) voltage is not small \( \rightarrow \) need to use the full model for the MOSFET

\( V_{DS} = V_{DD} - v_L > V_{DD} - v_L - V_{Th} - v_{GS} \rightarrow \text{saturated,} \)

as long as \( v_{GS} > V_{Th} \)

\[
\begin{align*}
    i_D &= \frac{\mu_n C_{ox}}{2} (W / L)(v_{GS} - V_{Th})^2 = K(V_{DD} - V_{Th} - v_L)^2 \\
    i_D(t) &= C_L \frac{dv_L}{dt} \\
    K(V_{DD} - V_{Th} - v_L)^2 &= C_L \frac{dv_L}{dt} dt \\
    &= \int_{t_0}^{t'} \frac{C_L}{K(V_{DD} - V_{Th} - v_L)^2} dv_L
\end{align*}
\]
Solve for Load Voltage

\[ t = \int_0^t \frac{dV_L^{'}}{t} = \int_0^t \frac{C_L dV_L^{'}}{K(V_{DD} - V_{Th} - V_L^{'})} = -\frac{C_L}{K(V_{DD} - V_{Th} - V_L^{'})} - \frac{C_L}{K(V_{DD} - V_{Th})} \]

\[ t = \frac{C_L (V_{DD} - V_{Th}) - C_L (V_{DD} - V_{Th} - V_L)}{K(V_{DD} - V_{Th})(V_{DD} - V_{Th} - V_L)} = \frac{C_L V_L}{K(V_{DD} - V_{Th})(V_{DD} - V_{Th} - V_L)} \]

\[ t[K(V_{DD} - V_{Th})^2 - K(V_{DD} - V_{Th})V_L] = C_L V_L \]

\[ V_L (-Kt(V_{DD} - V_{Th}) - C_L) = -tK(V_{DD} - V_{Th})^2 \]

\[ V_L (t) = \frac{K(V_{DD} - V_{Th})^2 t}{K(V_{DD} - V_{Th}) + C_L} \]

\[ \quad = \frac{[i_D(t = 0)]t}{1 + \left(\frac{1}{C_L} \frac{i_D(t = 0)}{V_{DD} - V_{Th}}\right)t} \]

Sampled Voltage Waveform

\[ V_L(t) = 1.5 V \]

Less than \( V_{DD} \)

Slope = \( i_D(t = 0)/C_L \)

\[ V_L \text{ approaches } V_{DD} - V_{Th} = 1.5 V \text{ (for } V_S = V_{DD}) \]

\[ \mu_n C_{ox} = 50 \mu A/V^2, (W/L) = 100 \rightarrow i_D(t = 0) = 5.6 mA \]
Improved Sample and Hold

NMOS and PMOS transistors in parallel \( \rightarrow \) sampled voltage can be pulled up to the supply voltage and pulled down to ground.