Announcements
- Homework 3, due today
- Homework 4 due next week
- Lab 2 this week
- Reading: Chapter 4

Lecture Material
- Last lecture
  - Diode currents
  - MOS capacitor
- This lecture
  - MOS transistor
  - Models

MOS CV Curve
- Small-signal capacitance is slope of Q-V curve
- Capacitance is linear in accumulation and inversion
- Capacitance is depletion region is smallest
- Capacitance is non-linear in depletion

C-V Curve Equivalent Circuits
- \( C_{ox} \)
- \( C_{ds} \)
- \( C_{gd} \)
- \( C_{gs} \)
- \( C_{ap} \)
- \( C_{aq} \)
\[
C_{aq} = \frac{\varepsilon_s}{x_{aq}} \quad C_{ap} = \frac{C_{aq}C_{gs}}{C_{gs} + C_{as}} = \frac{C_{aq}C_{gs}}{1 + C_{aq}C_{gs}/C_{gs}} = \frac{C_{aq}}{1 + \frac{C_{aq}}{C_{gs}}x_{aq}}
\]
- In accumulation mode the capacitance is just due to the voltage drop across \( x_{aq} \)
- In inversion the incremental charge comes from the inversion layer (depletion region stops growing).
- In depletion region, the voltage drop is across the oxide and the depletion region

MOSFET Cross Section
- Add two junctions around MOS capacitor
- The regions forms PN junctions with substrate
- MOSFET is a four terminal device
- The body is usually grounded (or at a DC potential)
- For ICs, the body contact is at surface
MOSFET Layout

- Planar process: complete structure can be specified by a 2D layout
- Design engineer can control the transistor width \( W \) and \( L \)
- Process engineer controls \( t_{ox}, N_a, x_j \), etc.

PMOS & NMOS

- A MOSFET by any other name is still a MOSFET:
  - NMOS, PMOS, nMOS, pMOS
  - NFET, PFET
  - Other flavors: JFET, MESFET
- CMOS technology: The ability to fabricated NMOS and PMOS devices simultaneously

CMOS

- Complementary MOS: Both P and N type devices
- Create a n-type body in a p-type substrate through compensation. This new region is called a “well”.
- To isolate the PMOS from the NMOS, the well must be reverse biased (pn junction)

Circuit Symbols

- The symbols with the arrows are typically used in analog applications
- The body contact is often not shown
- The source/drain can switch depending on how the device is biased (the device has inherent symmetry)

Observed Behavior: \( I_D-V_{GS} \)

- Current zero for negative gate voltage
- Current in transistor is very low until the gate voltage crosses the threshold voltage of device (same threshold voltage as MOS capacitor)
- Current increases rapidly at first and then it finally reaches a point where it simply increases linearly

Observed Behavior: \( I_D-V_{DS} \)

- For low values of drain voltage, the device is like a resistor
- As the voltage is increases, the resistance behaves non-linearly and the rate of increase of current slows
- Eventually the current stops growing and remains essentially constant (current source)
If the gate is biased above threshold, the surface is inverted. This inverted region forms a channel that connects the drain and gate. If a drain voltage is applied positive, electrons will flow from source to drain.

The current in this channel is given by:

$$I_{ds} = -W_V Q_N$$

The charge proportional to the voltage applied across the oxide over threshold is

$$Q_x = C_{ox} (V_{gs} - V_{th})$$

$$I_{ds} = -W_V C_{ox} (V_{gs} - V_{th})$$

If the channel is uniform density, only drift current flows

$$v_i = -\mu F, \quad F = -\frac{V_{ds}}{L}$$

$$I_{ds} = \frac{W}{L} \mu C_{ox} (V_{gs} - V_{th}) V_{ds} \quad V_{gs} > V_{th} \quad V_{ds} = 100\text{mV}$$

Notice that in the linear region, the current is proportional to the voltage:

$$I_{ds} = \frac{W}{L} \mu C_{ox} (V_{gs} - V_{th}) V_{ds}$$

Can define a voltage-dependent resistor:

$$R_{eq} = I_{ds} = \frac{1}{\mu C_{ox} (V_{gs} - V_{th})} \left( \frac{L}{W} \right) = R \left( V_{gs} \right) \frac{L}{W}$$

This is a nice variable resistor, electronically tunable!

Approximate inversion charge $Q_N(y)$: drain is higher than the source $\Rightarrow$ less charge at drain end of channel

$$Q_N(y) \approx Q_N(y = 0) + Q_N(y = L)$$

$$Q_N(y = 0) = -C_{ox} (V_{gs} - V_{th})$$

$$Q_N(y = L) = -C_{ox} (V_{gd} - V_{th})$$

$$V_{gd} = V_{gs} - V_{ds}$$

$$V_{gs} > V_{th}$$

$$V_{ds} = 100\text{mV}$$
Average Inversion Charge

Source End

\[ Q_s(y) = -\frac{C_A(V_{gs} - V_f) + C_A(V_{gs} - V_f)}{2} \]

Drain End

\[ Q_d(y) = -C_A(V_{gs} - V_f) + C_A(V_{gs} - V_f) \]

\[ Q_y(y) = -\frac{C_A(V_f - V_f - 2V_f)}{2} - C_A(V_f - V_f) = C_A(V_f - V_f - V_f) \]

- Charge at drain end is lower since field is lower
- Simple approximation: In reality we should integrate the total charge minus the bulk depletion charge across the channel

Drift Velocity and Drain Current

"Long-channel" assumption: use mobility to find \( v \)

\[ v(y) = -\mu_f E(y) = -\mu_f (-\Delta V / \Delta y) = \frac{\mu_f V_{ds}}{L} \]

Substituting:

\[ I_s = -WvQ_s = W\mu_f \frac{V_{ds}}{L} C_A(V_{gs} - V_f - \frac{V_{ds}}{2}) \]

\[ I_d = \frac{W}{L} \mu C_A(V_{gs} - V_f - \frac{V_{ds}}{2}) \]

Inverted Parabolas

Square-Law Characteristics

Boundary: what is \( I_{ds, sat} \)?

The Saturation Region

When \( V_{ds} > V_{gs} - V_{th} \), there isn’t any inversion charge at the drain ... according to our simplistic model

Why do curves flatten out?

Square-Law Current in Saturation

Current stays at maximum (where \( V_{ds} = V_{gs} - V_{th} = V_{ds,sat} \))

\[ I_{ds,sat} = \frac{W}{L} \mu C_A(V_{gs} - V_f - \frac{V_{ds}}{2}) \]

Measurement: \( I_d \) increases slightly with increasing \( V_{ds} \) model with linear "fudge factor"

\[ I_{ds,sat} = \frac{W}{L} \mu C_A(V_{gs} - V_f)^2 (1 + AW_{ds}) \]

Pinching the MOS Transistors

- When \( V_{ds} > V_{ds,sat} \), the channel is "pinched" off at drain end (hence the name "pinch-off region")
- Drain mobile charge goes to zero (region is depleted), the remaining electric field is dropped across this high-field depletion region
- As the drain voltage is increases further, the pinch off point moves back towards source
- Channel Length Modulation: The effective channel length is thus reduced → higher \( I_{ds} \)
Short-Channel MOSFET Model

Channel (inversion) charge: neglect reduction at drain

Velocity saturation defines $V_{DS, SAT} = E_{sat} L = \text{constant}$

Drain current:

$$I_{D, SAT} = -WvQ_N = -W(v_{sat})[-C_{ox}(V_{GS} - V_Tn)]$$

$$|E_{sat}| = 10^4 \text{ V/cm, } L = 0.12 \mu m \Rightarrow V_{DS, SAT} = 0.12 \text{ V!}$$

$$I_{D, SAT} = v_{sat} W C_{ox}(V_{GS} - V_Tn)(1 + \lambda_p V_{DS})$$

"Linear" I-V Characteristics:
short-channel MOSFET

$I_D$ versus $V_{DS}$

<table>
<thead>
<tr>
<th>$V_{GS}$ (V)</th>
<th>$I_D$ (A)</th>
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</thead>
<tbody>
<tr>
<td>2.5</td>
<td>4.0 x 10^{-4}</td>
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<tr>
<td>2.0</td>
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</tr>
<tr>
<td>1.5</td>
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Long Channel

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Short Channel