Announcements

- Homework 3, due next week
- Reading: Chapter 3 (3.7-3.9)
Lecture Material

- Last lecture
  - PN junction
  - Diode capacitance
- This lecture
  - Diode currents
  - MOS capacitor

### Diode under Thermal Equilibrium

- **Minority Carrier Close to Junction**

  > Diffusion small since few carriers have enough energy to penetrate barrier
  > Drift current is small since minority carriers are few and far between: Only minority carriers generated within a diffusion length can contribute current
  > Important Point: Minority drift current independent of barrier!
  > Diffusion current strong (exponential) function of barrier
Reverse Bias

- Reverse Bias causes an increase in barrier to diffusion
- Diffusion current is reduced exponentially

![Diagram of Reverse Bias](image)

- Drift current does not change
- Net result: Small reverse current

Forward Bias

- Forward bias causes an exponential increase in the number of carriers with sufficient energy to penetrate barrier
- Diffusion current *increases* exponentially

![Diagram of Forward Bias](image)

- Drift current does not change
- Net result: Large forward current
Diode I-V Curve

Diode IV relation is an exponential function

This exponential is due to the Boltzmann distribution of carriers versus energy

For reverse bias the current saturates to the drift current due to minority carriers

Minority Carriers at Junction Edges

Minority carrier concentration at boundaries of depletion region increase as barrier lowers ... the function is

\[
\frac{p_n(x = x_n)}{p_p(x = -x_p)} = \left( \frac{\text{minority hole conc. on n-side of barrier}}{\text{majority hole conc. on p-side of barrier}} \right)
\]

\[
= e^{- \frac{(\text{Barrier Energy})}{kT}}
\]

\[
\frac{p_n(x = x_n)}{N_A} = e^{-\frac{q(\phi_B - V_D)}{kT}}
\]

(Boltzmann’s Law)
“Law of the Junction”

Minority carrier concentrations at the edges of the depletion region are given by:

\[
\begin{align*}
  p_n(x = x_n) &= N_A e^{-q(\phi_B - V_D)/kT} \\
  n_p(x = -x_p) &= N_D e^{-q(\phi_B - V_D)/kT}
\end{align*}
\]

Note 1: \(N_A\) and \(N_D\) are the majority carrier concentrations on the other side of the junction

Note 2: we can reduce these equations further by substituting \(V_D = 0\) V (thermal equilibrium)

Note 3: assumption that \(p_n \ll N_D\) and \(n_p \ll N_A\)

Minority Carrier Concentration

The minority carrier concentration in the bulk region for forward bias is a decaying exponential due to recombination
Steady-State Concentrations

Assume that none of the diffusing holes and electrons recombine → get straight lines ...

This also happens if the minority carrier diffusion lengths are much larger than $W_{n,p}$

Diode Current Densities

$$\frac{dn_p}{dx}(x) \approx n_{p0} e^{qV/kT} - n_{p0}$$

$$n_{p0} = \frac{n_i^2}{N_i}$$

$$J_{n}^{\text{diff}} = qD_n \frac{dn_p}{dx} \bigg|_{x=x_p} \approx q \frac{D_n}{W_p} n_{p0} \left( e^{qV/kT} - 1 \right)$$

$$J_{p}^{\text{diff}} = -qD_p \frac{dp_n}{dx} \bigg|_{x=x_n} \approx -q \frac{D_p}{W_n} p_{n0} \left( 1 - e^{qV/kT} \right)$$

$$J^{\text{diff}} = qn_i^2 \left( \frac{D_p}{W_n} + \frac{D_n}{W_p} \right) \left( e^{qV/kT} - 1 \right)$$
Fabrication of IC Diodes

- Start with p-type substrate
- Create n-well to house diode
- p and n+ diffusion regions are the cathode and anode
- N-well must be reverse biased from substrate
- Parasitic resistance due to well resistance

Diode Small Signal Model

- The I-V relation of a diode can be linearized

\[ I_D + i_D = I_S \left( e^{\frac{q(V_j + V_d)}{kT}} - 1 \right) \approx I_S e^{\frac{qV_j}{kT}} e^{\frac{qV_d}{kT}} \]

\[ e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \cdots \]

\[ I_D + i_D \approx I_D \left( 1 + \frac{q(V_j + V_d)}{kT} + \cdots \right) \]

\[ i_D \approx \frac{qV_d}{kT} = g_d V_d \]
Diode Capacitance

- We have already seen that a reverse biased diode acts like a capacitor since the depletion region grows and shrinks in response to the applied field. The capacitance in forward bias is given by

\[ C_j = A \frac{E_s}{X_{dep}} \approx 1.4C_{j0} \]

- But another charge storage mechanism comes into play in forward bias.
- Minority carriers injected into p and n regions “stay” in each region for a while.
- On average additional charge is stored in diode.

Charge Storage

- Increasing forward bias increases minority charge density.
- By charge neutrality, the source voltage must supply equal and opposite charge.
- A detailed analysis yields:

\[ C_d = \frac{1}{2} \frac{qL_d}{kT} \tau \]

(Time to cross junction (or minority carrier lifetime))
Diode Circuits

- Rectifier (AC to DC conversion)
- Average value circuit
- Peak detector (AM demodulator)
- DC restorer
- Voltage doubler / quadrupler / …

MOS Capacitor

- MOS = Metal Oxide Silicon
- Sandwich of conductors separated by an insulator
- “Metal” is more commonly a heavily doped polysilicon layer
  - n⁺ or p⁺ layer
- NMOS → p-type substrate, PMOS → n-type substrate
Under thermal equilibrium, the n-type poly gate is at a higher potential than the p-type substrate.

\[ \phi_p = -\frac{kT}{q} \ln \frac{N_a}{n_i} \]

\[ \phi_{n^+} \approx 550 \text{mV} \]

No current can flow because of the insulator but this potential difference is accompanied with an electric field.

Fields terminate on charge!

At equilibrium there is an electric field from the gate to the body. The charges on the gate are positive. The negative charges in the body come from a depletion region.
Good Place to Sleep: Flat Band

If we apply a bias, we can compensate for this built-in potential:

\[ V_{FB} = -(\phi_n - \phi_p) \]

In this case the charge on the gate goes to zero and the depletion region disappears.

In solid-state physics lingo, the energy bands are “flat” under this condition.

Accumulation

If we further decrease the potential beyond the “flat-band” condition, we essentially have a parallel plate capacitor.

Plenty of holes and electrons are available to charge up the plates.

Negative bias attracts holes under gate.
Depletion

Similar to equilibrium, the potential in the gate is higher than the body

Body charge is made up of the depletion region ions

Potential drop across the body and depletion region

Inversion

As we further increase the gate voltage, eventually the surface potential increases to a point where the electron density at the surface equals the background ion density

\[ n_s = n_i e^{\frac{\phi_s}{kT}} = N_a \]

\[ \phi_s = -\phi_p \]

At this point, the depletion region stops growing and the extra charge is provided by the inversion charge at surface
Threshold Voltage

- The threshold voltage is defined as the gate-body voltage that causes the surface to change from p-type to n-type.
- For this condition, the surface potential has to equal the negative of the p-type potential.
- We'll derive that this voltage is equal to:

\[
V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2q\epsilon_s N_a (-2\phi_p)}
\]

Inversion Stops Depletion

- A simple approximation is to assume that once inversion happens, the depletion region stops growing.
- This is a good assumption since the inversion charge is an exponential function of the surface potential.
- Under this condition:

\[
Q_G(V_{Tn}) \approx -Q_{B,max}
\]

\[
Q_G(V_{GB}) = C_{ox}(V_{GB} - V_{Tn}) - Q_{B,max}
\]
Q-V Curve for MOS Capacitor

- In accumulation, the charge is simply proportional to the applies gate-body bias.
- In inversion, the same is true.
- In depletion, the charge grows slower since the voltage is applied over a depletion region.

Numerical Example

- MOS Capacitor with p-type substrate:
  \[
  t_{ox} = 20\text{nm} \quad N_a = 5 \times 10^{16} \text{ cm}^{-3}
  \]
- Calculate flat-band:
  \[
  V_{FB} = -(\phi_n - \phi_p) = -(550 - (-402)) = -0.95 \text{V}
  \]
- Calculate threshold voltage:
  \[
  C_{ox} = \frac{E_{ox}}{t_{ox}} = \frac{5.45 \times 10^{-13} \text{ F/cm}}{2 \times 10^6 \text{cm}}
  \]
  \[
  V_{Th} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2q\varepsilon_s N_a (-2\phi_p)}
  \]
  \[
  V_{Th} = -0.95 - 2(-0.4) + \frac{\sqrt{2 \times 1.6 \times 10^{-19} \times 1.04 \times 10^{-12} \times 5 \times 10^{16} \times 2 \times 0.4}}{C_{ox}} = 0.52 \text{V}
  \]
Num Example: Electric Field in Oxide

- Apply a gate-to-body voltage:
  \[ V_{GB} = -2.5 < V_{FB} \]

- Device is in accumulation
- The entire voltage drop is across the oxide:
  \[ E_{ax} = \frac{V_{ax}}{t_{ax}} = \frac{V_{GB} + \phi_s - \phi_p}{t_{ax}} = \frac{-2.5 + 0.55 - (-0.4)}{2 \times 10^{-6}} = -8 \times 10^5 \text{ V/cm} \]

- The charge in the substrate (body) consists of holes:
  \[ Q_B = -C_{ox} (V_{GB} - V_{FB}) = 2.67 \times 10^{-7} \text{ C/cm}^2 \]

Numerical Example: Depletion Region

- In inversion, what’s the depletion region width and charge?
  \[ V_{B,\text{max}} = \phi_s - \phi_p = -\phi_p - \phi_p = -2\phi_p = 0.8 \text{ V} \]
  \[ V_{B,\text{max}} = \frac{1}{2} \left( \frac{qN_a}{\varepsilon_s} \right) X_{d,\text{max}}^2 \]
  \[ X_{d,\text{max}} = \sqrt{\frac{2\varepsilon_s V_{B,\text{max}}}{qN_a}} = 144 \text{ nm} \]
  \[ Q_{B,\text{max}} = -qN_a X_{d,\text{max}} = -1.15 \times 10^{-7} \text{ C/cm}^2 \]