Announcements

- Lab 9 reports due now!
  - Check your homework/lab grades next week!
- Reading: Chapter 9.6, 10.7.2
- Final: December 20, 12:30-3:30pm, Bechtel Aud. (Sibley)
Lecture Material

- Last lecture
  - BJT amplifiers: common emitter, common collector, common base
- This lecture
  - BJT biasing
  - Example amplifier
  - Review

PNP Transistor

![PNP Transistor Diagram]
Multi-Stage Voltage Amplifier

Cutting Through the Complexity

Two Approaches:

1. Eliminate “background” transistors to reduce clutter

2. Identify the “signal path” between the input and output
First Approach: Find $I$ & $V$ Sources

What’s Left?

Voltage at base of $Q_2$ is set by totem pole
Second Approach: Find Signal Path

First stage (or two stages): CS/CB cascode
Second stage (or two stages): CD/CC voltage buffer

Why does this make sense for a voltage amplifier?
Find Key Two-Port Parameters

Output resistance of cascode:

\[ R_{out,CS/CB} = r_{oc} \parallel \left\{ r_{o2}(1 + g_{m2}(r_{\pi2} \parallel R_{S2})) \right\} \]

\[ r_{oc} = R_{up} = r_{o6}(1 + g_{m6}R_{S6}) \]
Output Resistance and Voltage Gain

Source resistance of the CC stage is the output resistance of the CD stage (small)

\[ R_{out} = R_{out,CC} = \frac{1}{g_{m4}} \frac{R_{S,CC}}{\beta_o} = \frac{1}{g_{m4}} \frac{1}{g_{m3} \beta_o} \approx \frac{1}{g_{m4}} \]

Open-circuit voltage gain \( A_v \) (last two stages have nearly unity gain):

\[ A_v = -g_{m1} (\beta_0 r_0 \| r_0 (1 + g_m 6 r_0 )) \]

Output Swing: \( V_{OUT,\text{MIN}} \)

Minimum output voltage: \( M_{10}, M_3, \) and \( Q_2 \) are “suspects”

- \( M_{10} \) goes into triode when \( V_{OUT} = 0.5 \text{ V} \)
- \( M_3 \) goes into triode when \( V_{SD3} = 0.5 \text{ V} \rightarrow V_{OUT} = 0.5 \text{ V} - 0.7 \text{ V} = -0.2 \text{ V} \)
- \( Q_2 \) goes into saturation when \( V_{CE2} = 0.1 \text{ V} \)
  - or \( V_{BC2} = 0.6 \text{ V} \)
  - \( V_{OUT} = V_{B2} - V_{BC2} + V_{SG3} - V_{BE4} = 2 \text{ V} - 0.6 \text{ V} + 1.5 \text{ V} - 0.7 \text{ V} \)
  - \( V_{OUT} = 2.2 \text{ V} \)
Output Swing: $V_{OUT,\text{MAX}}$

Maximum output voltage: $Q_4$, $M_5$, and $M_6$ are “suspects”

$Q_4$ goes into saturation when $V_{CE4} = 0.1 \text{ V} \rightarrow V_{OUT} = 4.9 \text{ V}$

$M_5$ goes triode when $V_{SD5} = 0.5 \text{ V} \rightarrow V_{OUT} = 3.8 \text{ V}$

$M_6$ goes triode when $V_{SD6} = 0.5 \text{ V} \rightarrow$

$V_{OUT} = V_{S6} - 0.5 \text{ V} + V_{SG3} - V_{BE4}$

$= 3.5 - 0.5 + 1.5 - 0.7 \text{ V} = 3.8 \text{ V}$

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Insight into the Frequency Response
Qualitative Insight

Could always do “brute force” open-circuit time constants

CS*-CB is a wideband stage ... so is the CD-CC buffer

Look for large \( R_{Tx} C_x \) products: high-impedance nodes are likely candidates

Node X

“High impedance node” is node X ... look at \( R_{Tx} C_x \)

Capacitance:

\[ C_x = C_{gd6} + C_{\mu 2} + C_{gd3} + C_{M3} \]

Miller for CD stage \((M_3)\)
Finding the Miller Capacitance $C_{M3}$

Gain across $C_{gs3}$:  
$$A_{VCgs3} = \frac{R_{L3}}{1/g_{m3} + R_{L3}}$$

$$R_{L3} = R_{in4} =$$

Dominant Pole of Voltage Amplifier

Thévenin resistance for $C_X$:  
$$R_{TX} = R_{out2} \parallel R_{in3} = R_{out, CB} \parallel R_{in, CD}$$

$$R_{TX} = r_{oc} \parallel r_{o2}(1 + g_{m2}(r_{\pi2} \parallel R_{S2})) \approx r_{o6}(1 + g_{m6}r_{o7}) \parallel r_{o2}\beta_0$$

Dominant pole:  
$$\omega_1^{-1} \approx R_{TX}C_X$$
Example: Cell Phone