Gain-Bandwidth Product

Result from Miller:

\[ \omega_p^{-1} \approx (R_s)C_{gs} + (1 + g_m R'_{out})C_{gd} \]

Low-frequency gain:

\[ A_{vo} = \frac{V_{out}}{V_s} \bigg|_{R_s R_L} = -g_m R'_{out} \]

Announcements

- Homework 10 due on Tuesday
- Lab 8 this week
  - Friday is a University holiday (no lab/discussion)
  - Friday’s lab 8 on November 18
  - No new lab next week
- Midterm 2 next Thursday, Nov. 17, 6:30-8pm, Sibley
  - Review session on Tuesday, Nov. 15, 6:30-8pm, 277 Cory
- Reading: Chapter 9 (9.1, 9.3, 9.5)

Lecture Material

- Last lecture
  - Time constants
- This lecture
  - Common drain, common gate frequency response
  - Multistage amplifiers

Gain-Bandwidth Product

Considering only the first pole (assuming zero and 2nd pole are at much higher frequencies):

For common-source amplifier:

\[ |A_{v0}|_{\omega_p} = \frac{g_m R'_{out}}{R_s C_{gs} + (1 + g_m R'_{out}) C_{gd}} \]

Special case: \( R_s \approx R_L < R_{oc}, r_{oc} \)

\[ |A_{v0}|_{\omega_p} \approx \frac{g_m R_L}{R_s C_{gs} + g_m R_L C_{gd}} \ll \omega_p \]

not that great!
Common-Drain Amplifier

\[ V_{DD} \]

\[ R_s \]

\[ R_L \]

\[ + \]

\[ v_{OUT} \]

\[ -V_{SS} \]

\[ v_{GS} \]

\[ I_{CS} \]

\[ + \]

\[ vs \]

\[ - \]

Two-Port CD Model with Capacitors

Ignore \( g_{mb} \)

Find Miller capacitor for \( C_{gs} \) – note that the gate-source capacitor is between the input and output

Voltage Gain \( A_{V_{C_GS}} \) Across \( C_{gs} \)

\[ A_{V_{C_GS}} = \frac{R_{out}}{R_L + R_{out}} = 1 \]

Note: this voltage gain is neither the two-port gain nor the "loaded" voltage gain

\[ C_{in} = C_{gd} + C_M = C_{gd} + (1 - A_{V_{C_GS}}) C_{gs} \]

\[ C_{in} = C_{gd} + \frac{1}{1 + g_m R_L} C_{gs} \]

\[ C_{in} \approx C_{gd} \]

Bandwidth of CD Amplifier

Input low-pass filter’s –3 dB frequency:

\[ \omega_p^{-1} = R_S \left( \frac{C_{gd}}{1 + g_m R_L} \right) \]

Substitute favorable values of \( R_S, R_L \):

\[ R_S \approx 1/g_m \quad R_L >> 1/g_m \]

\[ \omega_p^{-1} = (1/g_m) \left( C_{gd} + \frac{C_{gd}}{1 + 1/g_m} \right) = C_{gd}/g_m \]

\[ \omega_p = g_m / C_{gd} > \omega_T^+ \]

Bandwidth of the Common-Gate Amplifier

Two-Port CG Model with Capacitors

No Miller-transformed capacitor!

Unity-gain frequency is on the order of \( \omega_T \) for small \( R_L \)
**Summary of Single-Stage Amplifiers**

- **CS**: suffers from Miller-magnified capacitor for high-gain case
- **CD**: Miller transformation → nulled capacitor → “wideband stage”
- **CG**: no “Millerized” capacitor → wideband stage (for low load resistance)

**Multistage Amplifiers**

Necessary to meet typical specifications for any of the 4 types

We have 2 flavors (NMOS, PMOS) of each CS, CG, and CD

What are the constraints?

1. Input/output resistance matching
2. DC coupling (no passive elements to block the signal) … why not?

**Bandwidth of a Cascaded Stages**

Assume identical stages, same dominant pole, $\omega_p$

$$A_{TOT}(j\omega) = \left(\frac{A_0}{1 + \frac{j\omega}{\omega_p}}\right)^N$$

$$|A_{TOT}| = \left(\frac{|A_0|}{\sqrt{1 + \left(\frac{\omega_{BW}}{\omega_p}\right)^2}}\right)^N \frac{1}{\sqrt{2}} = \left(\frac{A_0}{\sqrt{1 + \left(\frac{\omega_{BW}}{\omega_p}\right)^2}}\right)^N$$

$$\frac{\omega_{BW}}{\omega_p} = \sqrt{\frac{2N-1}{N}}$$

- $N = 2$ $\omega_{BW} = 0.64\omega_p$
- $N = 3$ $\omega_{BW} = 0.51\omega_p$

**Using CMOS Stages**

Input resistance:

Voltage gain (2-port parameter):

Output resistance:

**Start: Two-Stage Voltage Amplifier**

- Use two-port models to explore whether the combination "works"

Results: $R_{in} = R_{in1}, R_{out} = R_{out2}, A_v =$

**Multistage Current Buffers**

Are two cascaded common-gate stages better than one?

Input resistance: $R_{in} = R_{in3}$
Summary of Cascaded Amplifiers

General goals:
1. Boost the gain parameter (except for buffers)
2. Optimize the input and output resistances

\[ R_{in} \quad R_{out} \]

Voltage:
Current:
Transconductance:
Transresistance:

Second Design Issue: DC Coupling

Constraint: large inductors and capacitors are not available
Output of one stage is directly connected to the input of the next stage \( \rightarrow \) must consider DC levels … why?

Alternate CS-CS Cascade

Use a PMOS CS Stage:

Complete Amplifier

CG Cascade: DC Biasing

Two stages can have different supply currents

CG Cascade: Sharing a Supply

First stage has no current supply of its own \( \rightarrow \) its output resistance is modified
The Cascode Configuration

Common source / common gate cascade is one version of a cascode (all have shared supplies)

DC bias:

Two-port model: first stage has no current supply of its own

Cascode Two-Port Model

Output resistance of first stage = \( R_{\text{out,CS}} = R_{\text{down,CS}} = r_{s1} \)

\[ R_{\text{out,CS}} = r_{s2} \parallel (1 + g_m C_{gs}) r_{s2} \]

\[ G_m = g_m \]

\[ R_s = \infty \]

Why is the cascode such an important configuration?

Miller Capacitance of Input Stage

Find the Miller capacitance for \( C_{gds1} \)

Input resistance to common-gate second stage is low \( \rightarrow \) gain across \( C_{gds1} \) is small.

Two-Port Model with Capacitors

Miller capacitance:

\[
C_M = (1 - A_{\text{voc_{gd1}}} C_{gd1})
\]

\[
A_{\text{voc_{gd1}}} = \frac{1}{g_{m2} r_{s1}} \approx \frac{g_{m1}}{g_{m2}} = -1
\]

\[
C_M = 2 C_{gd1}
\]