Announcements

- Homework 5 due today
- Homework 6 due next Tuesday
- Lab 4 this week
- Reading: Chapter 4 (4.5-4.6), 8.3
- Midterm 1 in nine days
  - October 13, 6:30-8pm, Sibley
Lecture Material

- Last lecture
  - MOS amplifier example
  - MOSFET small-signal model
- This lecture
  - Finish MOSFET small-signal model
  - MOS current sources

Role of the Substrate Potential

Need not be the source potential, but $V_B < V_S$
Lower substrate potential, increased voltage across depletion region – increased bulk charge

Effect: changes threshold voltage, which changes the drain current ... substrate acts like a “backgate”

$$V_T = V_{T0} + \gamma \left( \sqrt{V_{SB} - 2\phi_p} - \sqrt{-2\phi_p} \right)$$
Role of the Substrate Potential

Effect: Modulates threshold (acts as a weak “backgate”)

\[ g_{mb} = \frac{\Delta i_D}{\Delta v_{BS}} = \left. \frac{\partial i_D}{\partial v_{BS}} \right|_Q \]

\[ Q = (V_{GS}, V_{DS}, V_{BS}) \]

Result:

\[ g_{ab} = \left. \frac{\partial i_D}{\partial v_{BS}} \right|_Q = \left. \frac{\partial i_D}{\partial V_{gs}} \frac{\partial V_{gs}}{\partial v_{BS}} \right|_Q = \frac{g_m}{2\sqrt{-V_{gs}^2 - 2\phi'}} \]

Four-Terminal Small-Signal Model

\[ i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \frac{1}{r_o} v_{ds} \]
MOSFET Capacitances in Saturation

Gate-source capacitance: channel charge is not controlled by drain in saturation.

Gate-Source Capacitance $C_{gs}$

Wedge-shaped charge in saturation $\rightarrow$ effective area is $(2/3)WL$
(see H&S 4.5.4 for details)

$$C_{gs} = (2/3)WLC_{ox} + C_{ov}$$

Overlap capacitance along source edge of gate $\rightarrow$

$$C_{ov} = L_DWC_{ox}$$

(Underestimate due to fringing fields)

$$C_{ovd} = C_{ov} \approx L_D WC_{ox}$$
Gate-Drain Capacitance $C_{gd}$

Not due to change in inversion charge in channel

Overlap capacitance $C_{ov}$ between drain and source is $C_{gd}$

Junction Capacitances

Drain and source diffusions have (different) junction capacitances since $V_{SB}$ and $V_{DB} = V_{SB} + V_{DS}$ aren’t the same

Complete model (without interconnects)
P-Channel MOSFET

Measurement of $-I_D$ versus $V_{SD}$, with $V_{SG}$ as a parameter:

Square-Law PMOS Characteristics

The formula is:

$$I_{SD} = \frac{V_{GS} - V_{TP}}{2}$$
Small-Signal PMOS Model

MOSFET SPICE Model

Many “levels” ... we will use the square-law
“Level 1” model
See H&S 4.6 + Spice refs. on reserve for details.

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.MODEL MODN NMOS LEVEL = 1 VTO = 1 KP = 70U LAMBDA = .033 GAMMA = .6
+ PHI = 0.8 TOX = 1.5E-10 CGDO = 5E-10 CGSO = 5E-10 CJ = 1E-4 CJSW = 5E-10
+ MJ = 0.5 PB = 0.95

.MODEL MODP PMOS LEVEL = 1 VTO = -1 KP = 25U LAMBDA = .333 GAMMA = .6
+ PHI = 0.8 TOX = 1.5E-10 CGDO = 5E-10 CGSO = 5E-10 CJ = 3E-4 CJSW = 3.5E-10
+ MJ = 0.5 PB = 0.95
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