Announcements

- Homework 5 due next Tuesday
- Lab 3 this week, Lab 4 next week
- Reading: Chapter 4 (4.5-4.6), 8.3
- Midterm 1 in two weeks
  - October 13, 6:30-8pm, Sibley

Lecture Material

- Last lecture
  - Sample and hold
  - MOS amplifier example
- This lecture
  - MOSFET small-signal model

There is a Better Way!

- What’s missing: didn’t include device output impedance or charge storage effects (must solve non-linear differential equations…)
- Approach 2. Do problem in two steps.
  - DC voltages and currents (ignore small signals sources): set bias point of the MOSFET … we had to do this to pick \( V_{GS} \) already
  - Substitute the small-signal model of the MOSFET and the small-signal models of the other circuit elements …
- This constitutes small-signal analysis

Large-Signal Analysis

An MOS Amplifier
Small-Signal Analysis

Step 1. Find DC Bias – ignore small-signal source

V_{GS} was found in Lecture 9

Step 2: Small-Signal Modeling

What are the small-signal models of the DC supplies?

Small-Signal Models of Ideal Supplies

Small-signal model:

\[ V_s = \frac{\partial V_{app}}{\partial V_{app}} = \infty \]

\[ r_{app} = 0 \]

\[ G_{supply} = \frac{\partial I_{sup}}{\partial V_{sup}} = 0 \]

\[ r_{app} = \infty \]

open

The Transconductance \( g_m \)

Defined as the change in drain current due to a change in the gate-source voltage, with everything else constant

\[ g_m = \frac{-W}{L} \left( \frac{\partial I_D}{\partial V_{GS}} \right) \]

\[ g_m = \frac{-W}{L} \left( \frac{\partial I_D}{\partial V_{GS}} \right) \]

Output Resistance \( r_o \)

Defined as the inverse of the change in drain current due to a change in the drain-source voltage, with everything else constant

\[ r_o = \frac{-1}{\frac{\partial I_D}{\partial V_{DS}}} \]

Evaluating \( r_o \)

\[ r_o = \frac{-1}{\frac{\partial I_D}{\partial V_{DS}}} \]
Total Small Signal Current

\[ i_{ds}(t) = I_{bs} + i_{ds} \]
\[ i_{ds} = g_m V_{gs} + \frac{1}{\lambda} V_{ds} \]

Transconductance
Conductance

Putting Together a Circuit Model

\[ i_{ds} = g_m V_{gs} + \frac{1}{r_g} V_{ds} \]

MOS Amplifier

1: DC solution
\[ I_D = 0.1mA \]
\[ V_{GS} = 1.32V, \ V_{DS} = 2.5V \]

2: Small signal
\[ g_m = \frac{2I_D}{V_{DS} - V_{TH}} = 0.82 \text{ms/V} \]
\[ \lambda = \frac{1}{I_{DS}} \rightarrow \infty \]

MOS Amplifier: Small-Signal

\[ V_{gs} = V_s \]
\[ i_d = g_m V_{gs} \]
\[ V_o = -i_d R_d \]
\[ A_v = \frac{V_o}{V_s} = -g_m R_d \]
\[ A_v = -15.6 \]

MOS Amplifier

Output resistance: typical value \( \lambda = 0.05 \text{ V}^{-1} \)
\[ \lambda = \frac{1}{I_{DS}} = 200 \Omega \]

Voltage gain:
\[ A_v = -\left( \frac{2 \cdot 0.1}{0.32} \right) (25 \parallel 200) = -14.3 \]

Output resistance lowers voltage gain

Input and Output Waveforms

Output small-signal voltage amplitude: 14 x 25 mV = 350
Input small-signal voltage amplitude: 25 mV
What Limits the Output Amplitude?

1. \( v_{OUT}(t) \) reaches \( V_{DD} \) or 0 \( \ldots \) or

2. MOSFET leaves constant-current region and enters triode region

\[
v_{csoe} = V_{DD}
v_{gsoe} = V_{gsoe, sat} = V_{gso} - V_{th} = 0.32V
v_{csoe} = V_{gsoe} - (V_{gso} - V_{th}) = 2.18V
\]

Optimum bias point \( V_o = \)

Role of the Substrate Potential

Need not be the source potential, but \( V_g < V_s \)
Lower substrate potential, increased voltage across depletion region – increased bulk charge

Effect: changes threshold voltage, which changes the drain current \( \ldots \) substrate acts like a “backgate”

\[
V_f = V_{gs} + \frac{r}{\sqrt{V_{ds}^2 - 2\phi_s - 2\phi_f}}
\]

Role of the Substrate Potential

Effect: Modulates threshold (acts as a weak “backgate”)

\[
g_{mh} = \frac{\Delta I_D}{\Delta V_{BS}} = \frac{\partial I_D}{\partial V_{BS}}|_Q
Q = (V_{gso}, V_{dso}, V_{bso})
\]

Result:

\[
g_m = -\frac{\partial V_{th}}{\partial V_{gs}} = -\frac{\partial V_{th}}{\partial V_{ds}} = -\frac{V_{th}}{2\sqrt{V_{ds}^2 - 2\phi_s}}
\]

Four-Terminal Small-Signal Model

\[
i_{ds} = g_m v_{gs} + g_{mh} v_{hs} + \frac{1}{r_o} v_{ds}
\]

MOSFET Capacitances in Saturation

Gate-source capacitance: channel charge is not controlled by drain in saturation.

\[
C_{gs} = (2/3)WL C_{ox} + C_{ov}
\]

Wedge-shaped charge in saturation \( \rightarrow \) effective area is \( (2/3)WL \)
(see H&S 4.5.4 for details)

\[
C_{ov} = L_D W C_{ox}
\]

Underestimate due to fringing fields
**Gate-Drain Capacitance \( C_{gd} \)**

*Not due to change in inversion charge in channel*

Overlap capacitance \( C_{ov} \) between drain and source is \( C_{gd} \)

**Junction Capacitances**

Drain and source diffusions have (different) junction capacitances since \( V_{SB} \) and \( V_{DS} = V_{SB} + V_{DS} \) aren’t the same

**Complete model (without interconnects)**

**P-Channel MOSFET**

Measurement of \( I_{DS} \) versus \( V_{SD} \) with \( V_{SG} \) as a parameter:

**Square-Law PMOS Characteristics**

**Small-Signal PMOS Model**

Many "levels" ... we will use the square-law "Level 1" model

See H&S 4.6 + Spice refs. on reserve for details.

**MOSFET SPICE Model**

MODEL BODY PMOS LEVEL = 1 VTO = 1 KP = 100 LAMBDA = 0.3 GAMMA = 6
+ PHI = 0.3 TOX = 1.5E-11 OXDO = 5E-10 OXCO = 5E-10 CI = 3E-4 CI2W = 3E-10
+ MJ = 0.5 PBJ = 0.5

MODEL MOD PPMOS LEVEL = 1 VTO = 0.1 KP = 250 LAMBDA = 433 GAMMA = 6
+ PHI = 0.3 TOX = 1.5E-11 OXDO = 5E-10 OXCO = 5E-10 CI = 3E-4 CI2W = 3E-10
+ MJ = 0.5 PBJ = 0.5