Lecture 23: Multistage Amps-Cascades and Cascodes

Prof. Niknejad
Lecture Outline

- Example 1: Cascodes Amp Design
- Example 2: Two Stage CS Amp
CG Cascade: DC Biasing

Two stages can have different supply currents

Extreme case: \( I_{B\text{IAS}2} = 0 \text{ A} \)
CG Cascade: Sharing a Supply

First stage has no current supply of its own → its output resistance is modified
The Cascode Configuration

Common source / common gate cascade is one version of a cascode (all have shared supplies)

DC bias:

Two-port model: first stage has no current supply of its own
Cascode Two-Port Model

Output resistance of first stage = \( R_{out,CS} = R_{down,CS} = r_{o1} \)

\[
R_{out} \approx r_{oc2} \parallel (1 + g_m r_{o1}) r_{o2}
\]

\[
G_m = g_{m1}
\]

\[
R_{in} = \infty
\]

Why is the cascode such an important configuration?
Miller Capacitance of Input Stage

Find the Miller capacitance for $C_{gd1}$

Input resistance to common-gate second stage is low → gain across $C_{gd1}$ is small.
Two-Port Model with Capacitors

\[ C_M = (1 - A_{vC_{gd1}})C_{gd1} \]

\[ A_{vC_{gd1}} = -g_{m1} \left( \frac{1}{g_{m2}} \parallel r_{o1} \right) \approx - \frac{g_{m1}}{g_{m2}} = -1 \]

\[ C_M = 2C_{gd1} \]
Generating Multiple DC Voltages

Stack-up diode-connected MOSFETs or BJTs and run a reference current through them → pick off voltages from gates or bases as references.
Multistage Amplifier Design Examples

Start with basic two-stage transconductance amplifier:

Why do this combination?
Current Supply Design

Output resistance goal requires large $r_{oc}$ →
use cascode current source
DC voltages must be set for the cascode current supply transistors $M_3$ and $M_4$, as well as the gate of $M_2$.

Why include $M_{2B}$?
Complete Amplifier Schematic

Goals: \( g_{m1} = 1 \text{ mS}, \)
\( R_{out} = 10 \text{ M}\Omega \)
Device Sizes

\( M_1: \) select \((W/L)_1 = 200/2\) to meet specified \(g_{m1} = 1 \text{ mS}\)  
\[ \Rightarrow \text{find } V_{BIAS} = 1.2 \text{ V} \]

Cascode current supply devices: select \(V_{SG} = 1.5 \text{ V}\)
\((W/L)_4 = (W/L)_{4B} = (W/L)_3 = (W/L)_{3B} = 64/2\)

\( M_2: \) select \((W/L)_2 = 50/2\) to meet specified \(R_{out} = 10 \text{ MΩ}\)
\[ \Rightarrow \text{find } V_{GS2} = 1.4 \text{ V} \]

Match \(M_2\) with diode-connected device \(M_{2B}\).

Assuming perfect matching and zero input voltage, what is \(V_{OUT}\)?
Output (Voltage) Swing

Maximum $V_{OUT}$
Minimum $V_{OUT}$
Two-Port Model

Find output resistance $R_{out}$

$\lambda_n = (1/20) \ V^{-1}, \ \lambda_n = (1/50) \ V^{-1}$ at $L = 2 \ \mu m \ \rightarrow$

$r_{on} = (100 \ \mu A / 20 \ V^{-1})^{-1} = 200 \ k\Omega, \ r_{op} = 500 \ k\Omega$

$g_{m2} = \frac{2I_{D2}}{V_{GS2} - V_{Tn}} = \frac{2(100 \mu A)}{1.4V - 1V} = 500 \mu S$

$g_{m3} = \frac{2(-I_{D3})}{V_{SG3} + V_{Tp}} = \frac{2(100 \mu A)}{1.5V - 1V} = 400 \mu S$

$R_{out} = r_{oc} \parallel r_{o2} (1 + g_{m2} R_{S2}) = r_{o3} (1 + g_{m3} R_{S3}) \parallel r_{o2} (1 + g_{m2} r_{o1})$
Voltage Transfer Curve

Open-circuit voltage gain: 

\[ A_v = \frac{v_{out}}{v_{in}} = -g_m R_{out} \]
Two-Stage Amplifier Topology

Direct DC connection: use NMOS then PMOS

\[ V^+ = +2.5 \text{ V} \]

\[ V^- = -2.5 \text{ V} \]
Assume that the reference is a “sink” set by a resistor.

Must mirror the reference current and generate a sink for $i_{SUP_2}$.
Use Basic Current Supplies

\[ V^+ = +2.5 \text{ V} \]

\[ V^- = -2.5 \text{ V} \]

Diagram with transistors and annotations:

- \( M_3 \), \( M_4 \), \( M_5 \), \( M_6 \), \( M_7 \)
- \( I_{REF} \), \( R_{REF} \)
- \( i_{SUP1} \), \( i_{SUP2} \)
- \( -I_{D5} \), \( I_{D7} \)
Complete Amplifier Topology

What’s missing? The device dimensions and the bias voltage and reference resistor.