Lecture 22: Multistage Amps

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Lecture Outline

- Finish Current Mirrors
- An Example Using Cascodes
- Multistage Amps
- Cascode Amplifier: Magic!
The Integrated “Current Mirror”

- $M_1$ and $M_2$ have the same $V_{GS}$
- If we neglect CLM ($\lambda=0$), then the drain currents are equal
- Since $\lambda$ is small, the currents will nearly mirror one another even if $V_{out}$ is not equal to $V_{GS1}$
- We say that the current $I_{REF}$ is mirrored into $i_{OUT}$
- Notice that the mirror works for small and large signals!
Current Mirror as Current Source

- The output current of $M_2$ is only weakly dependent on $v_{OUT}$ due to high output resistance of FET
- $M_2$ acts like a current source to the rest of the circuit
Small-Signal Resistance of \( I \)-Source

\[
\begin{align*}
R_{o1} & \quad g_m v_{gs1} \\
v_{gs1} & = v_{gs2} \\
g_m v_{gs2} & \quad R_{o2}
\end{align*}
\]
Improved Current Sources

Goal: increase $r_{oc}$

Approach: look at *amplifier* output resistance results … to see topologies that boost resistance

Looks like the output impedance of a common-source amplifier with source degeneration
**Effect of Source Degeneration**

- Equivalent resistance loading gate is dominated by the diode resistance ... assume this is a small impedance.
- Output impedance is boosted by factor \((1 + g_m R_S)\)
Cascode (or Stacked) Current Source

Insight: $V_{GS2} = \text{constant \ AND \ } V_{DS2} = \text{constant}$

Small-Signal Resistance $r_{oc}$:

$$R_o \approx (1 + g_m R_S) r_o$$

$$R_o \approx (1 + g_m r_o) r_o$$

$$R_o \approx g_m r_o^2 \gg r_o$$
**Drawback of Cascode I-Source**

Minimum output voltage to keep both transistors in saturation:

\[
V_{OUT,MIN} = V_{DS4,MIN} + V_{DS2,MIN}
\]

\[
V_{DS2,MIN} > V_{GS2} - V_T = V_{DSAT2}
\]

\[
V_{D4} > V_{DSAT2} + V_{GS4} = V_{GS2} + V_{GS4} - V_T
\]

\[
V_{OUT,MIN} = V_{GS2} + V_{GS4} - V_T
\]
Current Sinks and Sources

**Sink:** output current goes to ground  
**Source:** output current comes from voltage supply

![Diagrams showing sink and source circuits]
Current Mirrors

Idea: we only need one reference current to set up all the current sources and sinks needed for a multistage amplifier.
Multistage Amplifiers

Necessary to meet typical specifications for any of the 4 types

We have 2 flavors (NMOS, PMOS) of CS, CG, and CD and the npn versions of CE, CB, and CC (for a BiCMOS process)

What are the constraints?

1. Input/output resistance matching

2. DC coupling (no passive elements to block the signal)
Summary of Cascaded Amplifiers

General goals:

1. Boost the gain parameter (except for buffers)
2. Optimize the input and output resistances

<table>
<thead>
<tr>
<th></th>
<th>$R_{in}$</th>
<th>$R_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage:</td>
<td>$\infty$</td>
<td>0</td>
</tr>
<tr>
<td>Current:</td>
<td>0</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Transconductance:</td>
<td>$\infty$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Transresistance:</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
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Start: Two-Stage Voltage Amplifier

- Use two-port models to explore whether the combination "works"

Results of new 2-port:  \( R_{in} = R_{in1}, \ R_{out} = R_{out2} \)

\[
A_v = -G_{m1} \left( R_{in2} \parallel R_{out1} \right) \times \left( -G_{m2} R_{out2} \right) \\
A_v = G_{m1} G_{m2} \left( R_{in2} \parallel R_{out1} \right) \left( R_{out2} \right)
\]
Add a Third Stage: CC

Goal: reduce the output resistance
(important spec. for a voltage amp)

Output resistance:

\[
R_{out} = \frac{1}{g_{m3}} + \frac{R_S}{\beta} = \frac{1}{g_{m3}} + \frac{r_{o2} \parallel r_{oc2}}{\beta}
\]
Using CMOS Stages

\[ A_v = -g_{m1} \left( r_{o1} \parallel r_{oc1} \right) \times g_{m2} \left( -r_{o2} \parallel r_{oc2} \right) \]

Input resistance: \( \infty \)

Voltage gain (2-port parameter):

Output resistance:

\[ R_{out} = \frac{1}{g_m + g_{mb}} \]
Multistage Current Buffers

Are two cascaded common-base stages better than one?

Input resistance: $R_{in} = R_{in1}$
Two-Port Models

Output impedance of stage #1 (large)

\[ R_{out} = R_{out2} \cong r_{02} \left( 1 + g_m r_\pi \parallel R_{S2} \right) \parallel r_{oc2} \]

\[ R_{out} \cong r_{02} \left( g_m r_\pi \right) \parallel r_{oc2} = \left( \beta_o r_{o2} \right) \parallel r_{oc2} \]
Common-Gate 2\textsuperscript{nd} Stage

\[ R_{out} = R_{out2} \cong r_{02} \left( 1 + g_{m2} R_{S2} \right) \| r_{oc2} \]

\[ R_{out} = R_{out2} \cong r_{02} \left( 1 + g_{m2} r_{oi} \| r_{oc1} \right) \| r_{oc2} \]
Second Design Issue: DC Coupling

Constraint: large inductors and capacitors are not available

Output of one stage is directly connected to the input of the next stage → must consider DC levels … why?

![Diagram](image)
Alternative CG-CC Cascade

Use a PMOS CD Stage: DC level shifts upward

\[ I_{SUP1} \]

\[ 1.7 \text{ V} \]

\[ 3.2 \text{ V} \]

\[ 2.5 \text{ V} \]

\[ I_{SUP2} \]

\[ 5.0 \text{ V} \]

\[ 5.0 \text{ V} \]
CG Cascade: DC Biasing

Two stages can have different supply currents

Extreme case: $I_{BIAS2} = 0 \text{ A}$
CG Cascade: Sharing a Supply

First stage has no current supply of its own $\rightarrow$ its output resistance is modified.
The Cascode Configuration

Common source / common gate cascade is one version of a cascode (all have shared supplies)

DC bias:

Two-port model: first stage has no current supply of its own
Cascode Two-Port Model

\[ R_{out,CS^*} = R_{down,CS} = r_{o1} \]

\[ R_{out} \approx r_{oc2} \parallel (1 + g_m r_{o1}) r_{o2} \]

\[ G_m = g_{m1} \]

\[ R_{in} = \infty \]

Why is the cascode such an important configuration?
Miller Capacitance of Input Stage

Find the Miller capacitance for $C_{gd1}$

Input resistance to common-gate second stage is low $\Rightarrow$ gain across $C_{gd1}$ is small.
Two-Port Model with Capacitors

Miller capacitance: \( C_M = (1 - A_{vC_{gd1}})C_{gd1} \)

\[
A_{vC_{gd1}} = -g_{m1} \left( \frac{1}{g_{m2}} \parallel r_{o1} \right) \approx - \frac{g_{m1}}{g_{m2}} = -1
\]

\[ C_M = 2C_{gd1} \]
Generating Multiple DC Voltages

Stack-up diode-connected MOSFETs or BJTs and run a reference current through them → pick off voltages from gates or bases as references.
Multistage Amplifier Design Examples

Start with basic two-stage transconductance amplifier:

Why do this combination?
Two-Stage Amplifier Topology

Direct DC connection: use NMOS then PMOS

$V^+ = +2.5 \text{ V}$

$V^- = -2.5 \text{ V}$
Assume that the reference is a “sink” set by a resistor

Must mirror the reference current and generate a sink for \( i_{SUP_2} \)
Use Basic Current Supplies

\[ V^+ = +2.5 \text{ V} \]
\[ V^- = -2.5 \text{ V} \]
Complete Amplifier Topology

What’s missing? The device dimensions and the bias voltage and reference resistor

V\(^+\) = + 2.5 V

V\(^-\) = - 2.5 V