Lecture 21:
Voltage/Current Buffer Freq Response

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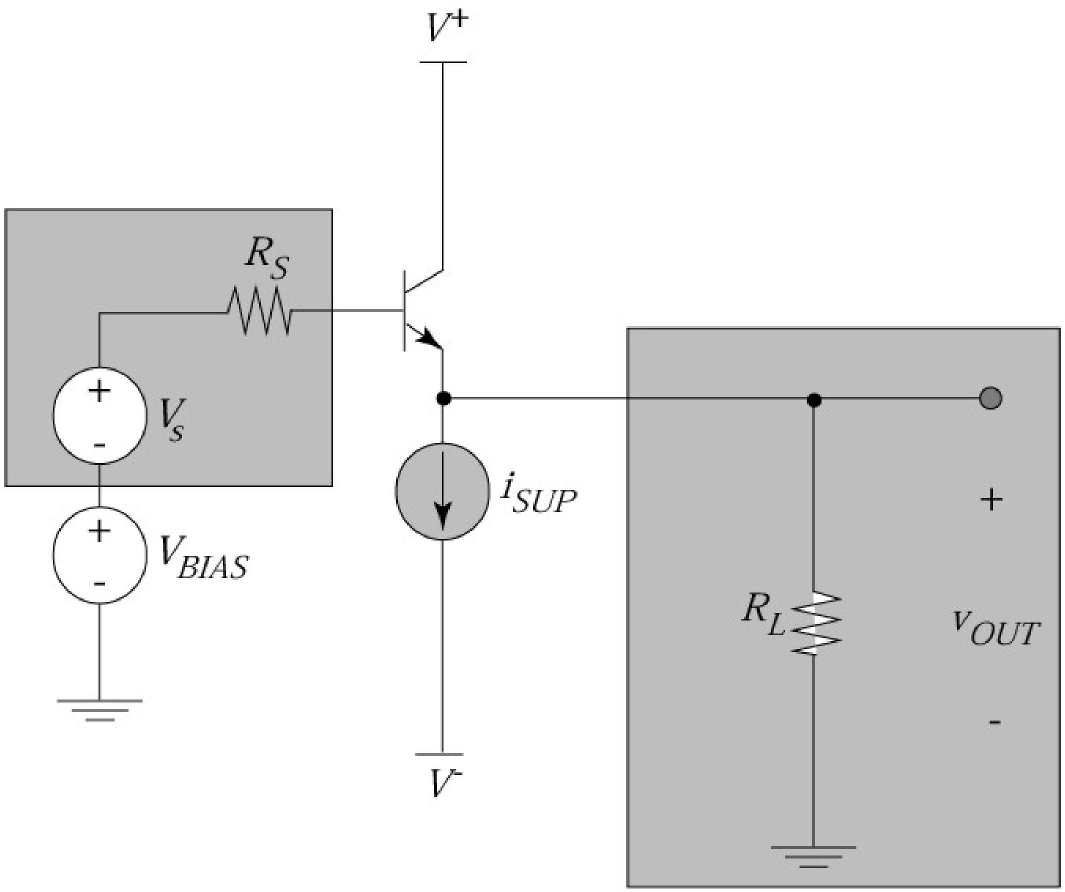
Lecture Outline

- Last Time: Frequency Response of Voltage Buffer
- Frequency Response of Current Buffer
- Current Mirrors
- Biasing Schemes
- Detailed Example

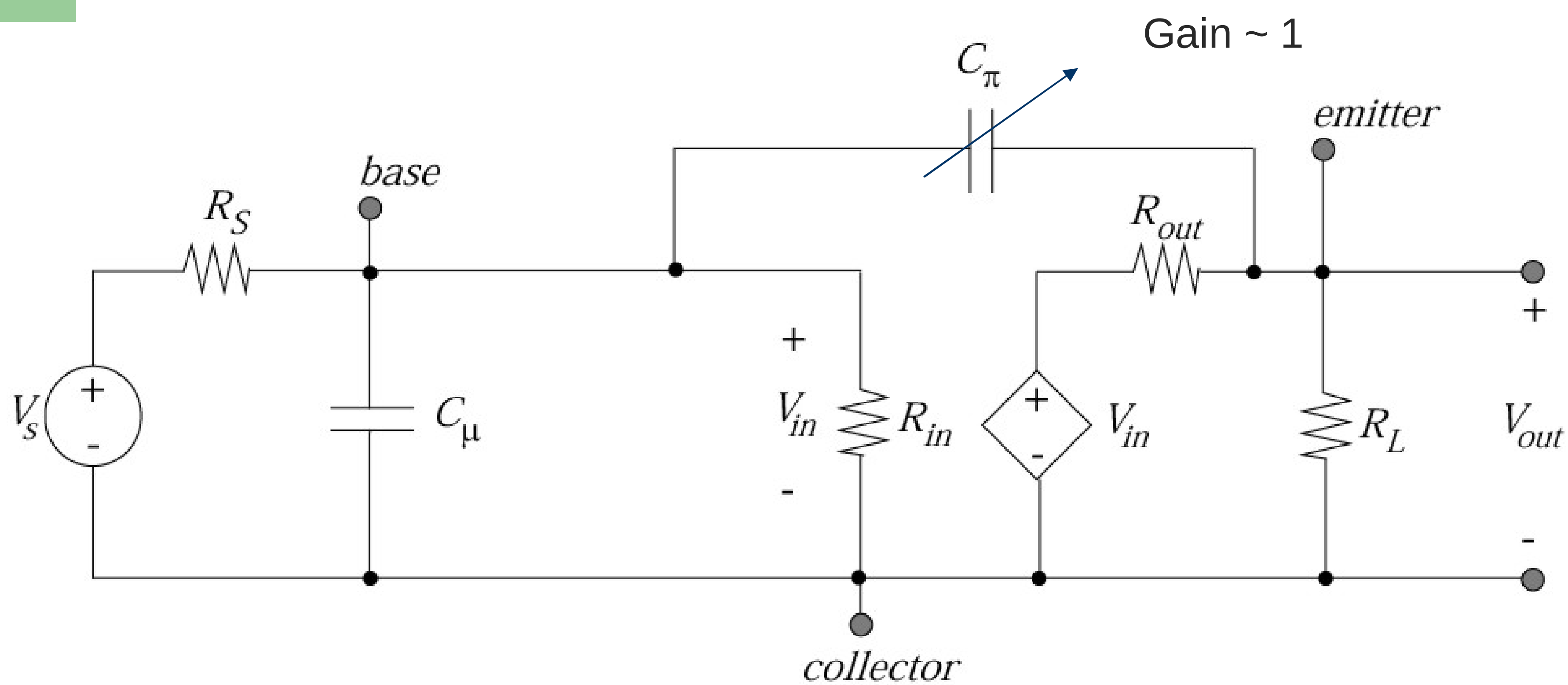
Common-Collector Amplifier



Procedure:

1. Small-signal two-port model
2. Add device (and other) capacitors

Two-Port CC Model with Capacitors



Find Miller capacitor for C_π -- note that the base-emitter capacitor is between the input and output

Voltage Gain $A_{vC\pi}$ Across C_π

$$A_{vC_\pi} \approx R_{out}/(R_{out}+R_L) \sim 1 \qquad R_{out} = \frac{1}{g_m}$$

$$g_m R_L >> 1$$

Note: this voltage gain is neither the two-port gain nor the "loaded" voltage gain

$$C_{in} = C_\mu + C_M = C_\mu + (1 - A_{vC_\pi})C_\pi$$

$$C_{in} = C_\mu + \frac{1}{1+g_m R_L} C_\pi$$

$$C_{in} \approx C_\mu$$

Bandwidth of CC Amplifier

Input low-pass filter's –3 dB frequency:

$$\omega_p^{-1} = \left(R_S \parallel R_{in}\right)\left(C_\mu + \frac{C_\pi}{1 + g_m R_L}\right)$$

Substitute favorable values of R_S, R_L:

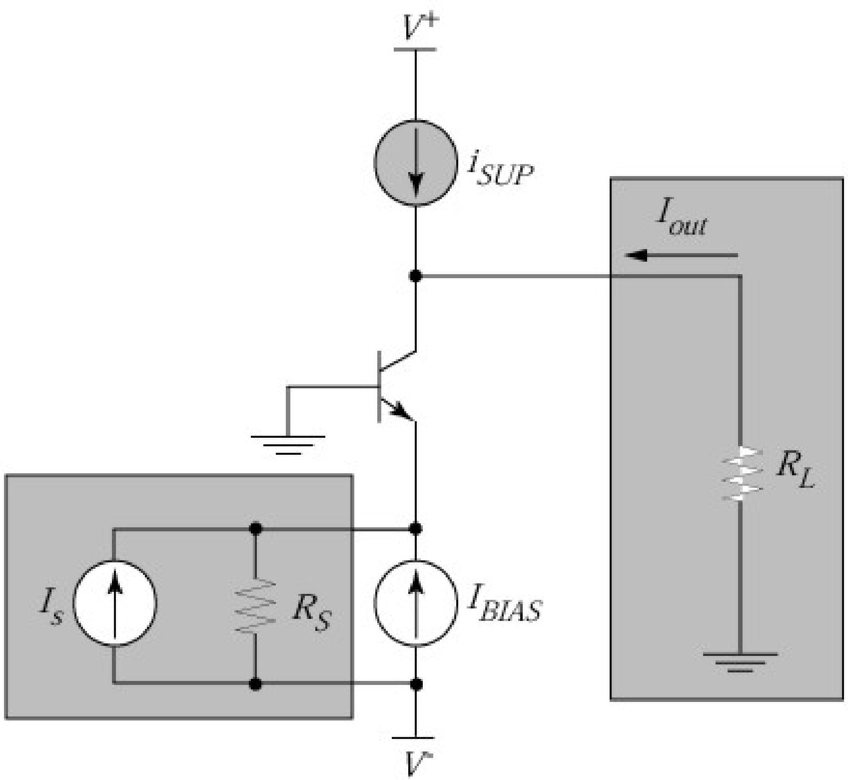
$$R_S \approx 1/g_m \qquad R_L >> 1/g_m$$

$$\omega_p^{-1} \approx \left(1/g_m\right)\left(C_\mu + \frac{C_\pi}{1 + BIG}\right) \approx C_\mu / g_m$$

$$\omega_p \approx g_m / C_\mu > \omega_T$$

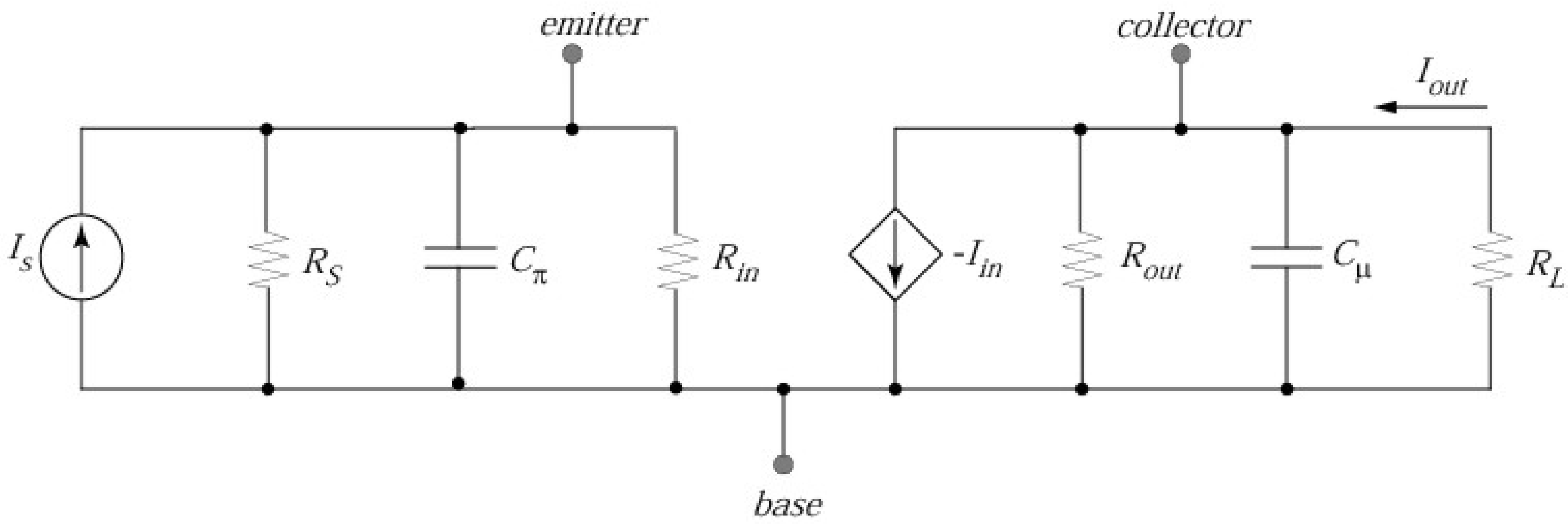
Model not valid at these high frequencies

CB Current Buffer Bandwidth



Same procedure: start with two-port model and capacitors

Two-Port CB Model with Capacitors



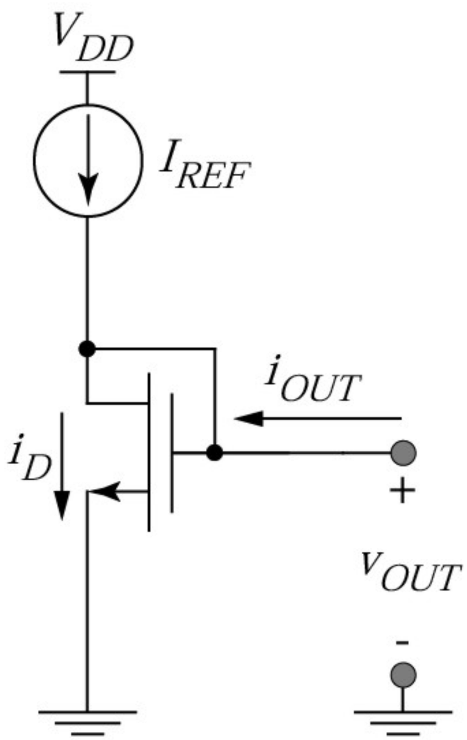
No Miller-transformed capacitor!

Unity-gain frequency is on the order of ω_T for small R_L

Summ of Single-Stage Amp Freq Resp

- CE, CS: suffer from Miller-magnified capacitor for high-gain case
- CC, CD: Miller transformation → nulled capacitor → "wideband stage"
- CB, CG: no Millerized capacitor → wideband stage (for low load resistance)

CMOS Diode Connected Transistor

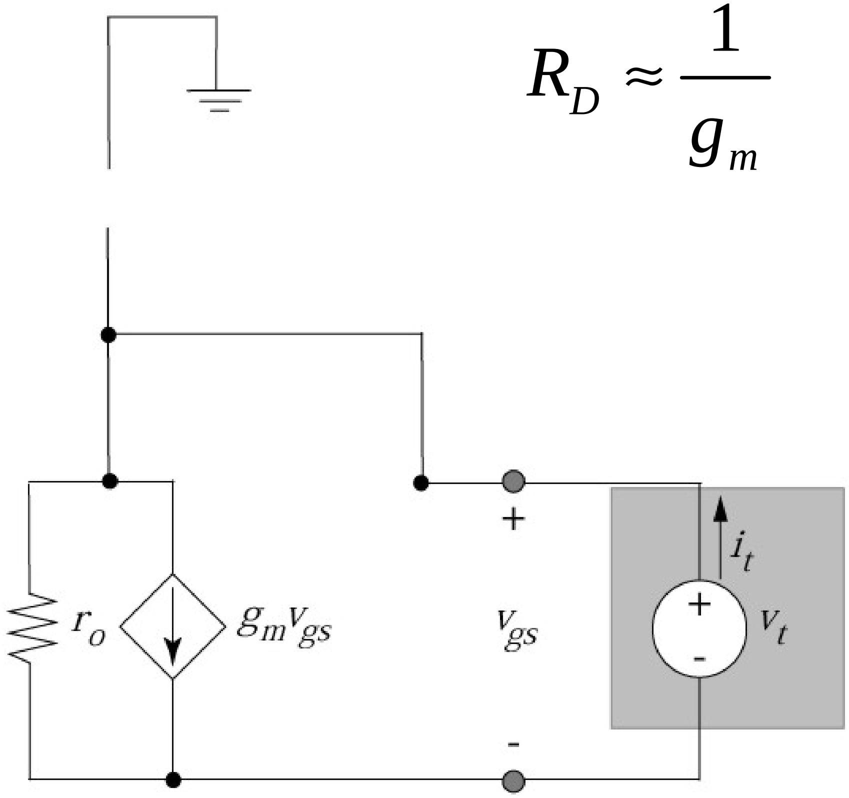


- Short gate/drain of a transistor and pass current through it
- Since VGS = VDS, the device is in saturation since VDS > VGS-VT
- Since FET is a square-law (or weaker) device, the I-V curve is very soft compared to PN junction diode
- What's the input impedance of circuit?

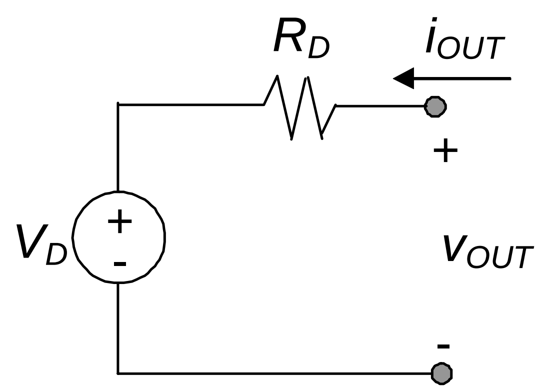
Diode Equivalent Circuit

$$R_D = \left(\left. \frac{di_{OUT}}{dv_{OUT}} \right|_{I_{OUT}=0} \right)^{-1} = \frac{v_t}{i_t}$$

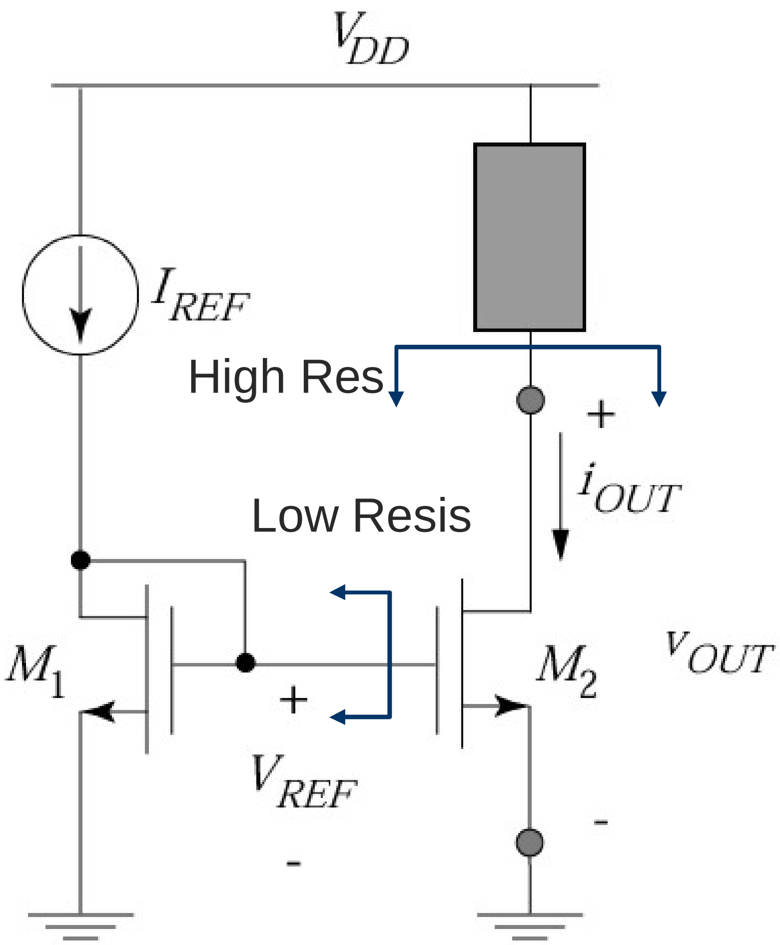
$$R_D \approx \frac{1}{g_m}$$



Equivalent Circuit:

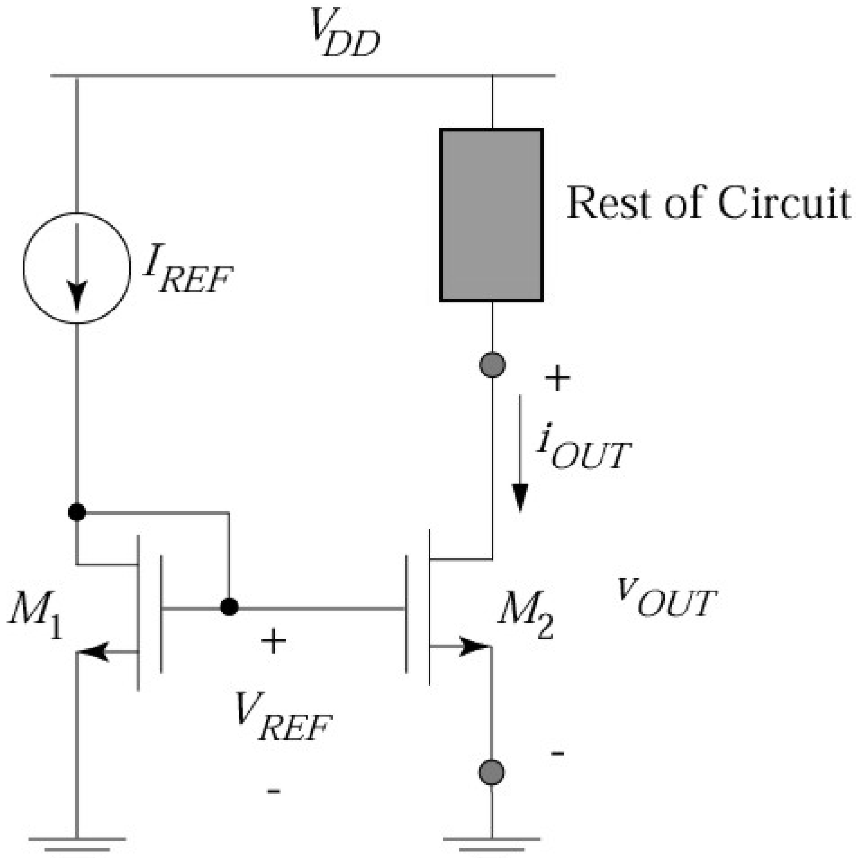


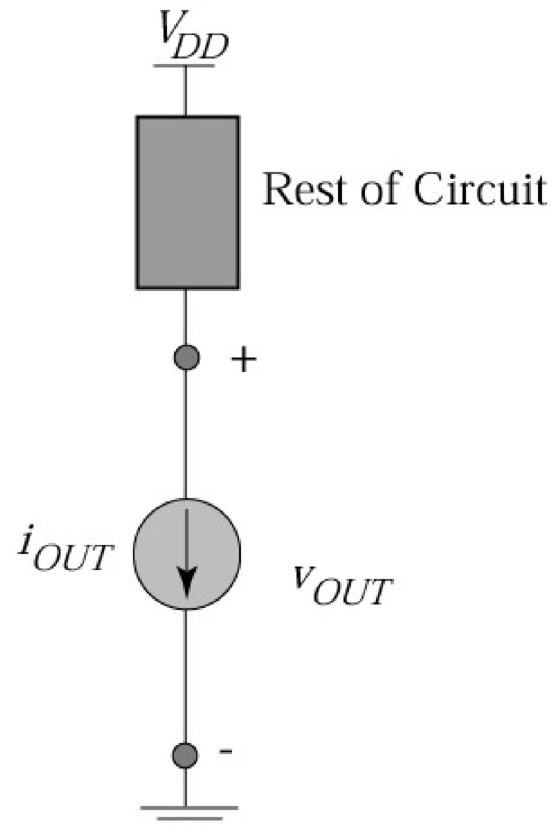
The Integrated "Current Mirror"



- M_1 and M_2 have the same V_{GS}
- If we neglect CLM (λ=0), then the drain currents are equal
- Since λ is small, the currents will nearly mirror one another even if V_{out} is not equal to V_{GS1}
- We say that the current I_{REF} is mirrored into i_{OUT}
- Notice that the mirror works for small and large signals!

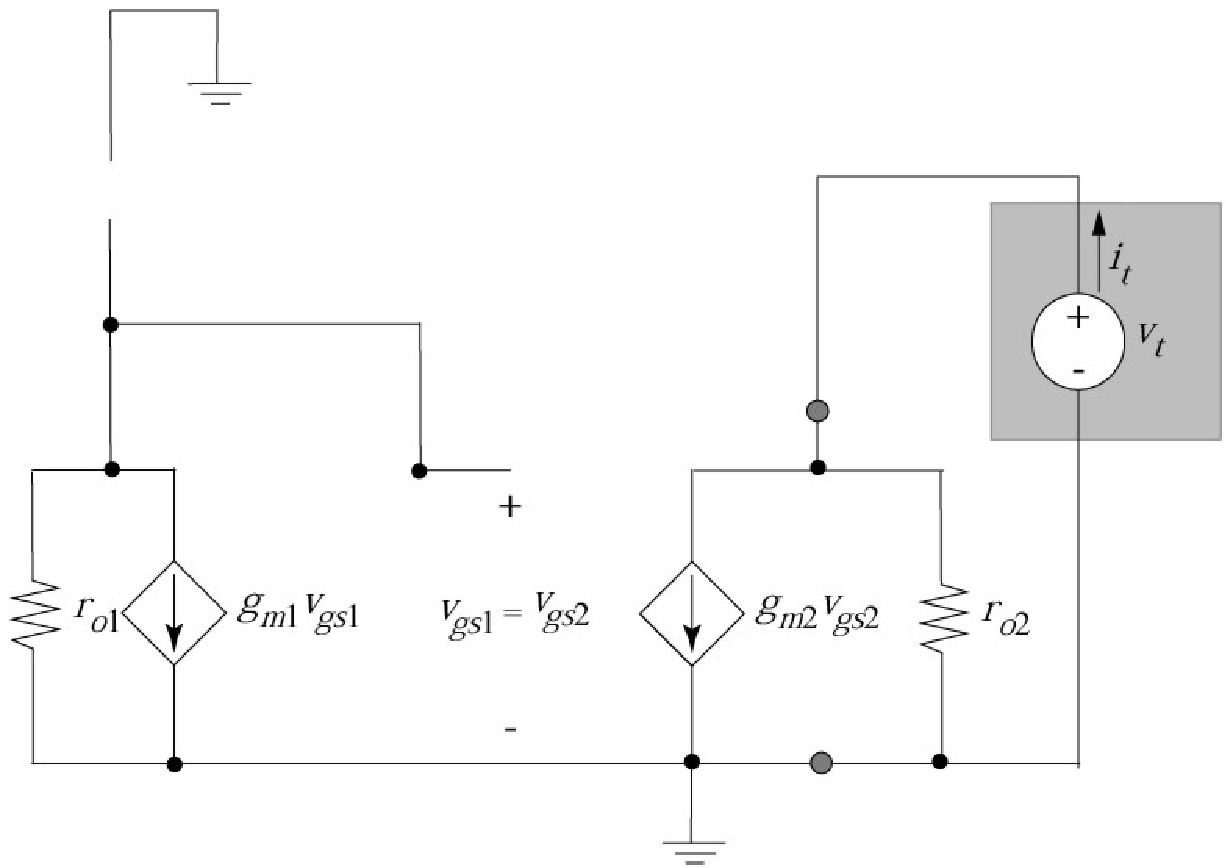
Current Mirror as Current Source





- The output current of M_2 is only weakly dependent on v_{OUT} due to high output resistance of FET
- M2 acts like a current source to the rest of the circuit

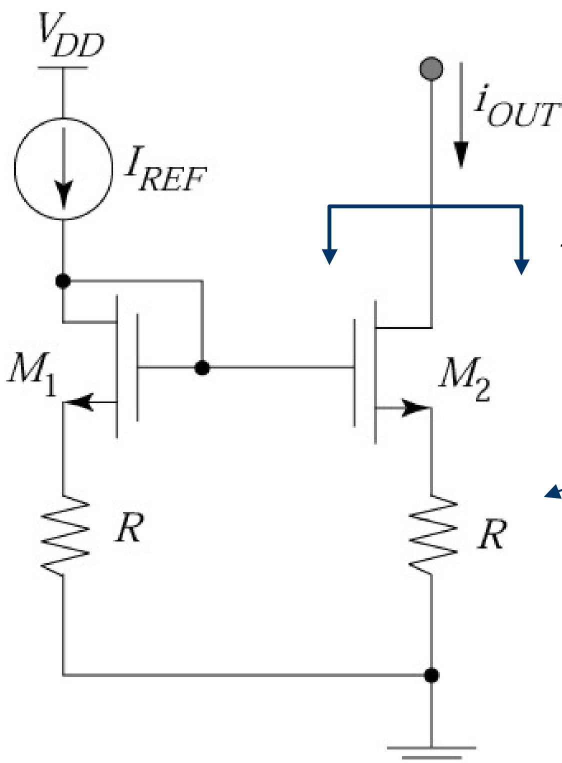
Small-Signal Resistance of *I*-Source



Improved Current Sources

Goal: increase r_{oc}

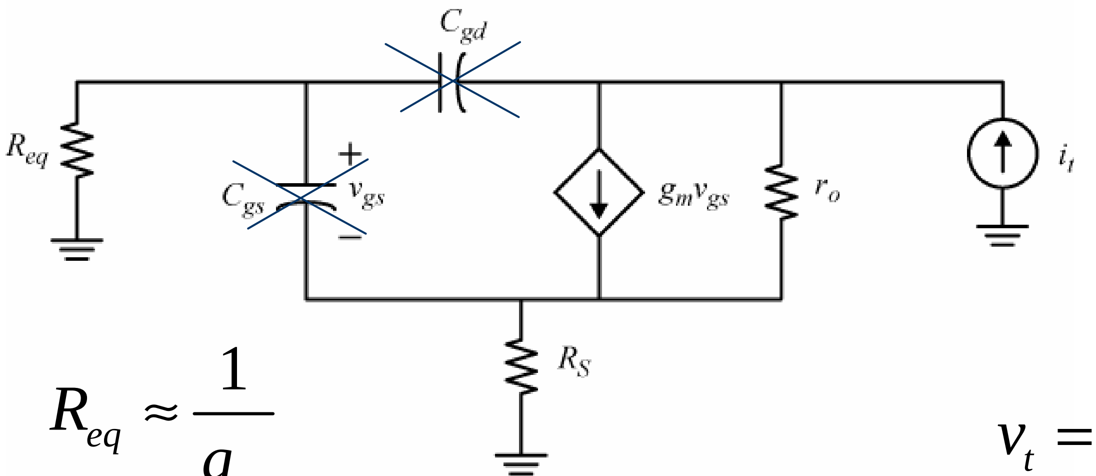
Approach: look at *amplifier* output resistance results … to see topologies that boost resistance



$R_{out} >> r_o$

Looks like the output impedance of a common-source amplifier with source degeneration

Effect of Source Degeneration



$$R_{eq} \approx \frac{1}{g_m}$$

$$v_t = (i_t - g_m v_{gs}) r_o + v_{R_S}$$

$$v_{gs} \approx -v_{R_S}$$

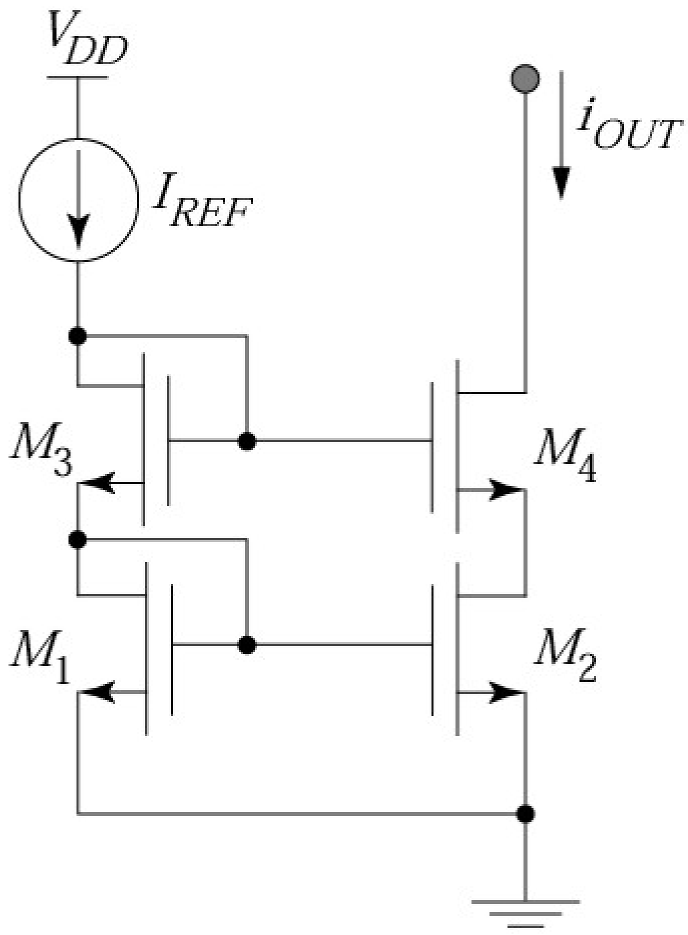
$$v_{R_S} = i_t R_S$$

$$v_t = (i_t + g_m R_S i_t) r_o + i_t R_S$$

$$R_o = \frac{v_t}{i_t} \approx (1 + g_m R_S) r_o$$

- Equivalent resistance loading gate is dominated by the diode resistance … assume this is a small impedance
- Output impedance is boosted by factor $(1 + g_m R_S)$

Cascode (or Stacked) Current Source



Insight: V_{GS2} = constant AND
V_{DS2} = constant

Small-Signal Resistance r_{oc}:

$$R_o \approx (1 + g_m R_S) r_o$$

$$R_o \approx (1 + g_m r_o) r_o$$

$$R_o \approx g_m r_0^2 >> r_o$$

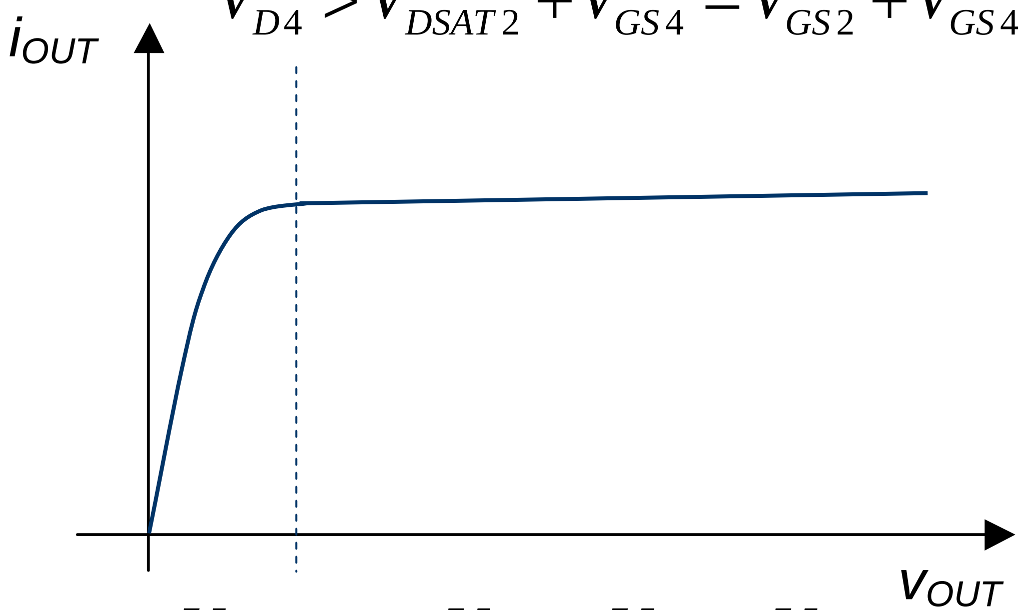
Drawback of Cascode *I*-Source

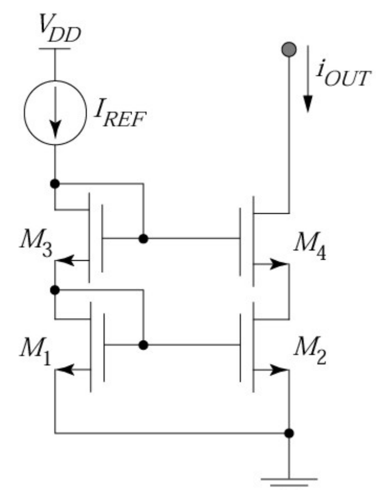
Minimum output voltage to keep both transistors in saturation:

$$V_{OUT,MIN} = V_{DS4,MIN} + V_{DS2,MIN}$$

$$V_{DS2,MIN} > V_{GS2} - V_{T0} = V_{DSAT2}$$

$$V_{D4} > V_{DSAT2} + V_{GS4} = V_{GS2} + V_{GS4} - V_{T0}$$





$$V_{OUT,MIN} = V_{GS2} + V_{GS4} - V_{T0}$$

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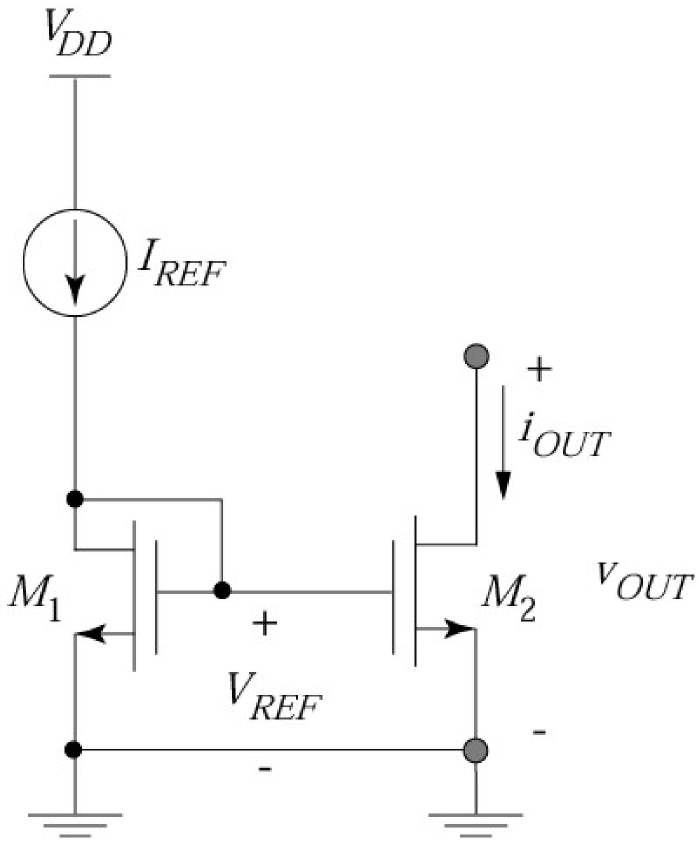
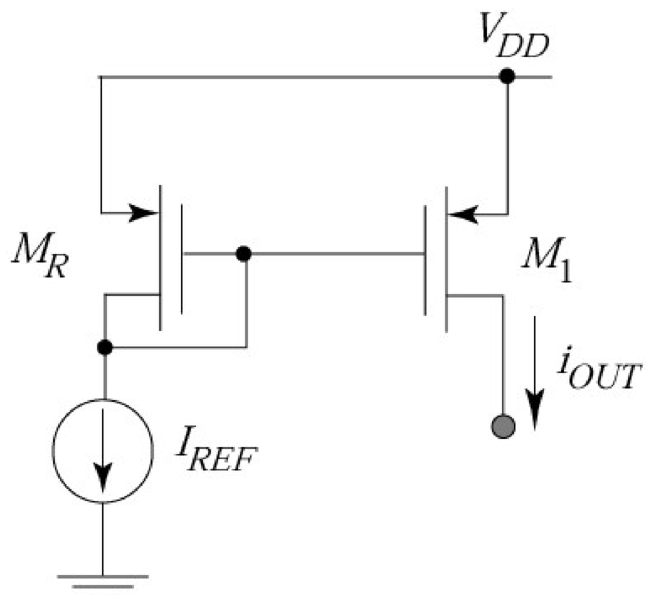
Current Sinks and Sources

Sink: output current goes to ground



Source: output current comes from voltage supply



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Current Mirrors

Idea: we only need one reference current to set up all the current sources and sinks needed for a multistage amplifier.