# Microelectronic Devices and Circuits- EECS105 

First Midterm Exam

Wednesday, October 6, 1999
Costas J. Spanos
University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

Your Name: $\qquad$

Your Signature: $\qquad$

1. Print and sign your name on this page before you start.
2. You are allowed a single, handwritten sheet with formulas. No books or notes!
3. Do everything on this exam, and make your methods as clear as possible.


## Problem 1 of 3. Answer each question briefly and clearly. ( 35 points)

What happens to $\mathrm{n}_{\mathrm{i}}$ if the temperature increases? Give a brief qualitative explanation (5pts)

What is the concentration of holes, electrons and positive/gnegative ions if Si is doped with $10^{17}$ Boron atoms $/ \mathrm{cm}^{3}$, and $10^{19}$ As atoms $/ \mathrm{cm}^{3}$ at room temperature? $\left(\mathrm{n}_{\mathrm{i}}=10^{10}\right)(5 \mathrm{pts})$

What are the three types of charges in an MOS capacitor under inversion? Mention carrier type (holes or electrons), ion polarity (positive or negative), charge nature (depletion, accumulation or inversion) and location (gate, substrate surface or bulk). (Gate is $n+$, bulk is $p) /(6 \mathrm{pts})$

Find the resistance of the following structure (drawn to scale), if the $\mathrm{Rs}_{1}$ (diffusion) is $20 \Omega /$ square, $\mathrm{Rs}_{2}$ (metal) is $1 \Omega /$ square and contact hole conductivity (i.e. the area where the two layers touch) is 1 Siemens $/ \mu \mathrm{m}^{2}$. (1Siemens $=1 / \Omega$ ) Assume that "dogbone" contact areas amount to 0.65 squares. (6pts)


What is the "law" of the junction? (5pts)

Sketch the minority charge concentration in the bulk of a pn junction under forward bias, and also under reverse bias (no need to calculate the width of the depletion regions - assume that the diode is "short"). (8pts):


## Problem 2 of 3 ( 40 points)

Follow these steps to create an MOS transistor:
0 . Start with p-type $10^{17} / \mathrm{cm}^{3}$ Boron susbstrate.

1. Grow $0.5 \mu \mathrm{~m}$ of $\mathrm{SiO}_{2}$ everywhere.
2. Use mask 1 to etch $\mathrm{SiO}_{2}$ where mask 1 is dark.
3. Grow 15 nm SiO 2 everywhere. (draw cross section after this step)
4. Deposit and pattern $0.5 \mu \mathrm{~m}$ of $\mathrm{n}+$ poly using mask 2 (poly remains where mask 2 is dark).
5. Implant $\mathrm{n}+$ regions (to make source and drain) in areas not covered by poly or thick $\mathrm{SiO}_{2}$. (draw cross section after this step).
6. The device is finished by cutting contact holes over source/drain, and by depositing oxide and patterning metal (contact hole and metal masks not shown) (10 points).


After the transistor has been completed, apply $\mathrm{V}_{\mathrm{DS}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{BS}}=0 \mathrm{~V}$, and $\mathrm{V}_{\mathrm{GS}}=\mathrm{V}_{\mathrm{tn} 0}$ to bring this device to the onset of inversion. Draw $\phi(\mathrm{x})$ (with reference to intrinsic silicon) and mark the values of $\mathrm{V}_{\mathrm{tn} 0}$, $\mathrm{X}_{\mathrm{dmax}} \cdot\left(\varepsilon_{\mathrm{o}}=8.85 \times 10^{-14} \mathrm{~F} / \mathrm{cm}, \varepsilon_{\mathrm{ox}}=3.9 \varepsilon_{0}, \varepsilon_{\mathrm{si}}=11.7 \varepsilon_{\mathrm{o}}\right.$, electron charge is $\left.-1.6 \times 10^{-19} \mathrm{Cb}\right)$ (10 points).


Apply $\mathrm{V}_{\mathrm{BS}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{DS}}=2 \mathrm{~V}, \mathrm{~V}_{\mathrm{GS}}=3 \mathrm{~V}$ and draw $\phi(\mathrm{x})$ at a spot very close to the source, and also at a spot very close to the drain. Draw both plots on the same graph, but mark each plot carefully. (Hint: the bulk potential stays the same, at $\phi_{\mathrm{p}}$ with reference to intrinsic silicon in both cases)(15 points).


Consider the small signal model for this transistor at $\mathrm{V}_{\mathrm{GS}}=2 \mathrm{~V}, \mathrm{~V}_{\mathrm{BS}}=0 \mathrm{~V}$. The large signal source $V_{C C}$ is such that the transistor is saturated. Calculate the values of $g_{m}$ and $r_{o}$ (assume $\mu_{\mathrm{n}}=215 \mathrm{~cm}^{2} \mathrm{~V}^{-1} \mathrm{~s}^{-1}$, and that the channel-length modulation parameter $\lambda_{\mathrm{n}}$ is $0.1 \mathrm{~V}^{-1}$ ). If we connect a small-signal source $\mathrm{v}_{\mathrm{gs}}=1 \mathrm{mV}$, what is the small signal voltage, $\mathrm{v}_{\text {out }}$, across $\mathrm{R}_{\mathrm{L}}=100 \mathrm{~K} \Omega$ connected as shown? (Do not take $\lambda_{\mathrm{n}}$ into account when you calculate $\mathrm{g}_{\mathrm{m}}$ ). ( 15 points)


## Problem 3 of 3 ( 25 points)

Consider a short pn junction with $\mathrm{I}_{\mathrm{o}}=10^{-9} \mathrm{~A}$. You want to make a thermometer out of this diode, by feeding it with a constant forward current of $10^{-3} \mathrm{~A}$, and by reading the bias voltage. What kind of function of temperature will be this voltage? (linear or some other kind?) Calculate the $\mathrm{V}_{\mathrm{D}}$ values for $0^{\circ} \mathrm{C}, 25^{\circ} \mathrm{C}$ and $100^{\circ} \mathrm{C}$. Graph the relationship between temperature and $\mathrm{V}_{\mathrm{D}}$. (Boltzman's constant is $1.3810^{-23} \mathrm{~J} / \mathrm{K}$. The absolute zero temperature is at $0^{\circ} \mathrm{K}$ or at $-273^{\circ} \mathrm{C}$.) ( 15 points)


How would a npn BJT be affected by the following parameters (draw up or down arrows to indicate that a parameter increases or decreases, respectively, given an increase of the respective design variable.) (10 points)

| Design Variable | $\beta_{\mathrm{F}}$ | $\alpha_{\mathrm{F}}$ |
| :--- | :--- | :--- |
| Emitter Doping |  |  |
| Emitter Width |  |  |
| Base Doping |  |  |
| Base Width |  |  |

