Microelectronic Devices and Circuits- EECS105

Second Midterm Exam

Wednesday, November 13, 2002

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Department of Electrical Engineering and Computer Sciences

Your Name: Official Solutions.
(last) (first)

Your Signature: _____

$n = 69$ $\hat{\mu} = 60$, $\hat{\sigma} = 18$

1. *Print and sign your name on this page before you start.*
2. *You are allowed two 8.5"x11" handwritten sheets with formulas. No books or notes!*
3. *Do everything on this exam, and make your methods as clear as possible.*

Problem 1	_____ / 35
Problem 2	_____ / 35
Problem 3	_____ / 30
TOTAL	_____ / 100

Problem 1 of 3 Answer each question briefly and clearly. Sketch a simple drawing if it helps you make your point. (35 points)

What is channel-length modulation, and how does it impact the behavior of a MOSFET? (5pts)

As V_{DS} increase, the depletion region around the drain increases and the channel gets shorter. As a result, I_D increases.

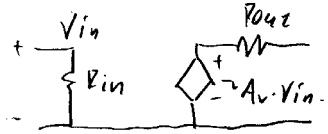
$$I_D = \frac{1}{2}\frac{W}{L}\mu_n C_{ox}(V_{TH}-V_{GS})^2(1+\lambda_n V_{DS})$$

↑ this is due to channel length modulation

Circle the most likely value for each of the following small signal parameters of a typical, silicon-based BJT(5pts)

r_o	10 Ω	10 kΩ	(100 kΩ)	10 MΩ
r_π	2.5 Ω	250 Ω	(25 kΩ)	2,5 MΩ
g_m	1 μS	(1 mS)	0.1 S	10 S

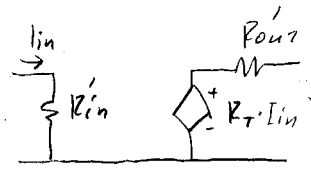
You are given a 2-port, which has R_{in}=1kΩ, R_{out}=100kΩ, and an open circuit voltage gain A_v = -10. Please draw the equivalent transresistance 2-port and calculate its R_{in}, R_{out}, and R_m. (5pts)



Voltage Amp.

$R_T \cdot I_{in} = (A_v \cdot V_{in}) = A_v \cdot I_{in} \cdot R_{in} \Rightarrow$

$R_T = A_v \cdot R_{in} = -10 \cdot 1K\Omega = -10K\Omega$



Voltage is proportional to input current (trans-resistance Amp)

$R'_{in} = R_{in} = 1K\Omega$ $R_{out}' = R_{out} = 100K\Omega$ R_T

What happens to the absolute, no-load (R_L infinity) voltage gain of a CS amplifier as you decrease the L of the transistor? Assume that he supply current stays the same.Provide a one sentence explanation or a formula to justify your answer (assuming that the bias current stays constant). (5 pts)

circle one: the absolute gain... increases (decreases) stays the same

and this is why:

$g_m \propto \sqrt{\frac{W}{L}}$ so, if L↓ then g_m ↑ by $\frac{1}{\sqrt{L}}$

$r_o = \frac{L}{\lambda I_D}$ so, if L↓ then r_o ↓ by L

} gain $\propto |g_m \cdot r_o|$ so gain ↓ by $\sqrt{L}$

What happens to the bandwidth of a CS amplifier as you decrease the L of the transistor? Provide a one sentence explanation or a formula to justify your answer (assuming that the bias current stays constant). (5 pts)

circle one: the bandwidth... (increases) decreases stays the same

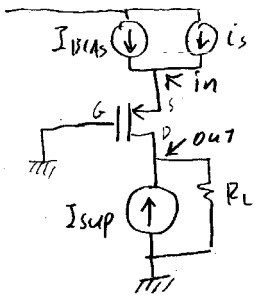
and this is why:

ultimately bandwidth is limited by $f_T \simeq \frac{1}{2\pi\tau_F}$

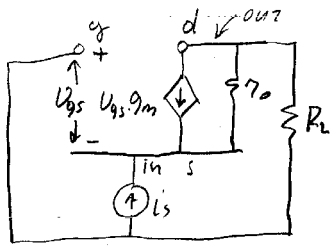
$\tau_F = \frac{L}{V_{sat}}$, so as L↓ τ_F↓ f_T↑

Sketch the large and small signal circuits of a CG amplifier utilizing a pmos transistor and an ideal current supply Isup. Include an ideal current source i_s as the input, and a load R_L. (5 pts)

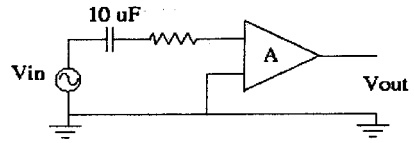
Large Signal



Small Signal



In the EE105 lab on amplifiers, a 10 μF capacitor is connected to the small-signal input voltage v_{in}. (See the following figure for a generic amplifier circuit.) What is the purpose of this capacitor? Why do we choose the capacitance to be so large? (5 pts)



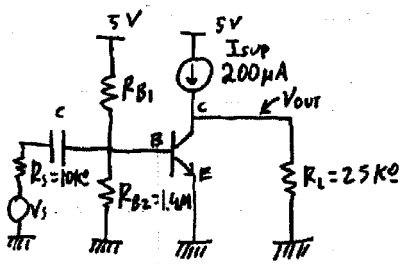
we use a huge C (10μF) to make sure that even low frequency signals go through.

We do not use a short because we want to block any DC voltage from going through.

Problem 2 of 3 (35 points)

For each of the following questions, make sure that you show the expressions before you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

Consider the following CE amplifier.



$\beta_o = 100$
$V_{th} = 26mV$
Assume that V_A and r_{oc} are infinite
Assume that $V_{BE\ on} = 0.7V$

$R_{B2} = 1.4M\Omega$
$R_s = 10k\Omega$
$R_L = 25k\Omega$
$I_{SUP} = 200\mu A$

a) Calculate the value of R_{B1} so that $V_{OUT} = 2.5V$. (15 points)

$V_{OUT} = 2.5V \rightarrow I_{R_L} = 100\mu A$

$I_{SUP} = I_C + I_{R_L} \rightarrow I_C = 100\mu A$

$I_C = \beta I_B \rightarrow I_B = 1\mu A$

$V_{BE} = V_{R_{B2}} = 0.7V \rightarrow I_{R_{B2}} = 0.5\mu A$

$I_{R_{B1}} = I_{R_{B2}} + I_B = 1.5\mu A$

$V_{R_{B1}} = 5V - V_{BE} = 4.3V$

$R_{B_1} = \frac{4.3V}{1.5\mu A} = 2.86\ M\Omega$

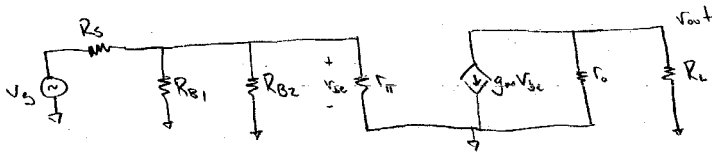
Final expression of R_{B1}:

$$R_{B1} = \frac{5V - V_{BE}}{\frac{V_{BE}}{R_{B2}} + \frac{I_{SUP} - \frac{V_{OUT}}{R_L}}{\beta}}$$

Calculated R_{B1} value:

2.86MΩ

b) Draw the small signal equivalent of this circuit, assuming that C is huge and therefore it can be replaced with a short circuit for small signal purposes. Ignore all other parasitic capacitors. Write the expression and calculate the small signal voltage gain v_{out} / v_s. (15 points)



$$v_{out} = g_m v_{be}(r_o // R_L) \qquad r_o = \infty$$

$$= g_m R_L \frac{(r_\pi // R_{B1} // R_{B2})}{R_S + (r_\pi // R_{B1} // R_{B2})} = \frac{g_m R_L}{1 + \left(\frac{1}{r_\pi} + \frac{1}{R_{B1}} + \frac{1}{R_{B2}}\right) R_S} = \frac{\frac{I_C}{V_{th}} R_L}{1 + \left(\frac{I_C}{\beta V_{th}} + \frac{1}{R_{B1}} + \frac{1}{R_{B2}}\right) R_S}$$

Final Expression of Voltage Gain v_{out} / v_s

$$\frac{-\frac{I_C}{V_{th}} R_L}{1 + \left(\frac{I_C}{\beta V_{th}} + \frac{1}{R_{B1}} + \frac{1}{R_{B2}}\right) R_S}$$

Calculated value of v_{out}/v_s

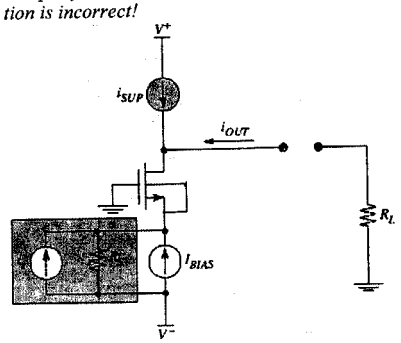
-70.8

c) There is something obviously inefficient with the way this amplifier is biased. Can you point to the problem and explain how you would fix it? (Here I expect a verbal explanation - not any quantitative analysis). (5 points)

Half of the supply current is constantly being burned in the load resistor. We could avoid this problem if we used a coupling capacitor on the output as well as on the input. That would allow the signal current to flow into the load but prevent DC current from flowing into it.

Problem 3 of 3 (30 points)

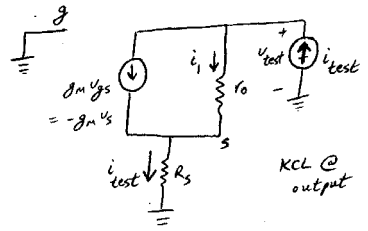
For each of the following questions, make sure that you show the expressions before you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!



$V_{Tn} = 1V$
$\mu_n C_{ox} = 50\mu A/V^2$
$\lambda_n = 0.1V^{-1}$ µm / L (where L in µm)
$-I_{BIAS} = Isup = 100\mu A$
r_{oc} is infinite (i.e. i_{SUP} is an ideal current source)
$R_S = 1k\Omega$
$R_L = 100k\Omega$

a) We need to design this amplifier so that $R_{in\ max} = 100\Omega$, and $R_{out,\ min} = 10M\Omega$. Calculate the minimum W and the minimum L of this transistor. (Note that these specs are very aggressive, so this will not turn out to be a "typical" MOS transistor with "typical" values.) (20 pts)

R_{out}



$v_s = i_{test} R_s$

$\therefore -g_m v_s = -g_m i_{test} R_s$

$i_1 = \dfrac{v_{test} - v_s}{r_o} = \dfrac{v_{test} - i_{test} R_s}{r_o}$

KCL @ output : $i_{test} + g_m v_s = i_1$

$\therefore i_{test} + g_m i_{test} R_s = \dfrac{v_{test} - i_{test} R_s}{r_o}$

$\therefore \dfrac{v_{test}}{i_{test}} = R_{out} = r_o + R_s + g_m R_s r_o \approx r_o(1 + g_m R_s)$

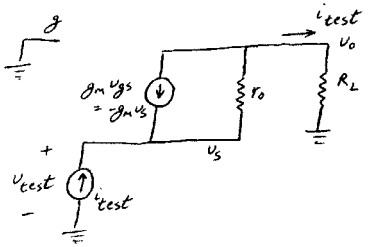
Write Expression for the minimum W/L here

$$\frac{W}{L} = \frac{1}{2 R_{in}^2 \mu C_{ox} I_D}$$ since $R_{in} \approx 1/g_m$ w/ $R_{in} = 100$

Value of min W/L

10,000

R_{in}



$v_o = i_{test} R_L$ (1)

KCL @ input :

$i_{test} = g_m v_s + \dfrac{v_s - v_o}{r_o}$

Using (1) and noting $v_s = v_{test}$

$i_{test} = g_m v_{test} + \dfrac{v_{test} - i_{test} R_L}{r_o}$

$\therefore \dfrac{v_{test}}{i_{test}} = R_{in} = \dfrac{r_o + R_L}{g_m r_o + 1} \approx \dfrac{1}{g_m}$

Now, $r_o = \dfrac{L}{\lambda I_D}$ and $g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D}$

w/ $I_D = 100\mu$, and setting $R_{in} = 100\ \Omega$

$R_{out} = 10\ M\Omega$

$L \approx 9\ \mu m$

$W \approx 91 \times 10^3\ \mu m$

Write Expression for minimum L here

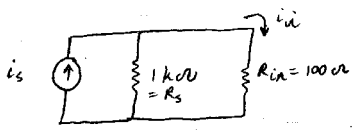
R_{out}

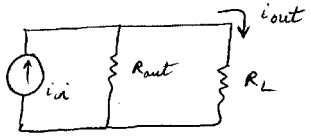
$$L = \frac{(10\,M\Omega)\lambda I_D}{(1+g_m R_s)}$$

Value of min L

$\approx 9\,\mu m$

b) Calculate the overall (loaded) current gain, (note that V_{bs}=0V) i_{out} / i_s.(10pts)





$$i_i = i_s \frac{R_s}{R_s + R_{in}}$$

$$i_{out} = i_i \frac{R_{out}}{R_{out} + R_L}$$

$$\therefore A_i = \frac{i_{out}}{i_s} = \frac{i_i}{i_s} \cdot \frac{i_{out}}{i_i} = \frac{R_s}{R_s + R_{in}} \frac{R_{out}}{R_{out} + R_L}$$

Write Expression for i_{out}/i_s here

Value of i_{out}/i_s

≈ 0.9