University of California at Berkeley
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 105 Practice Midterm I

Fall 2001 Prof. Roger T. Howe

Guidelines

Closed book and notes; one 8.5" x 11" page (both sides) of *your own notes* is allowed.
You may use a calculator.
Do not unstaple the exam.
Show all your work and reasoning on the exam in order to receive full or partial credit.

The exam will have 50 points and last 80 minutes, so you should time the sample problems at 1.6 minutes per point.

Exam Coverage

Lectures 1-13, Problem Sets 1-5, and related material in the textbook.

Midterm Review Session

Monday, Oct. 8, 2001, 6:00 – 7:30 pm, 277 Cory Hall

Solutions to sample midterm problems will be distributed and discussed at the review session; they will be also be available in 497 Cory Hall on Tuesday morning, Oct. 9.

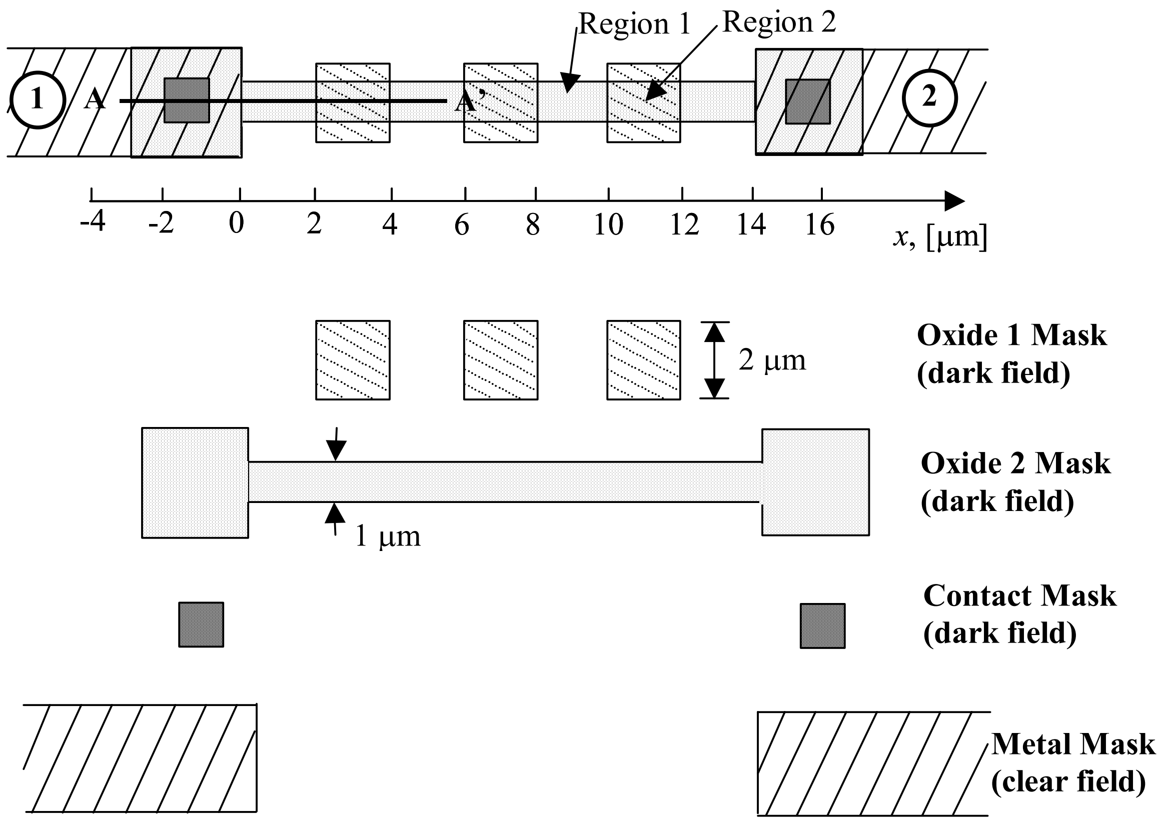
Midterm Exam

Wednesday, Oct. 10, 2001, 6:00 – 7:30 pm, Sibley Auditorium

Midterm Office Hours

RTH ***Teaching Assistants: TBA***
Monday, October 8, 1:15 – 3:30
Tuesday, October 9, 10:30 – 12:00, 2:00 – 3:00

1. Integrated Circuit Resistor [17 points]

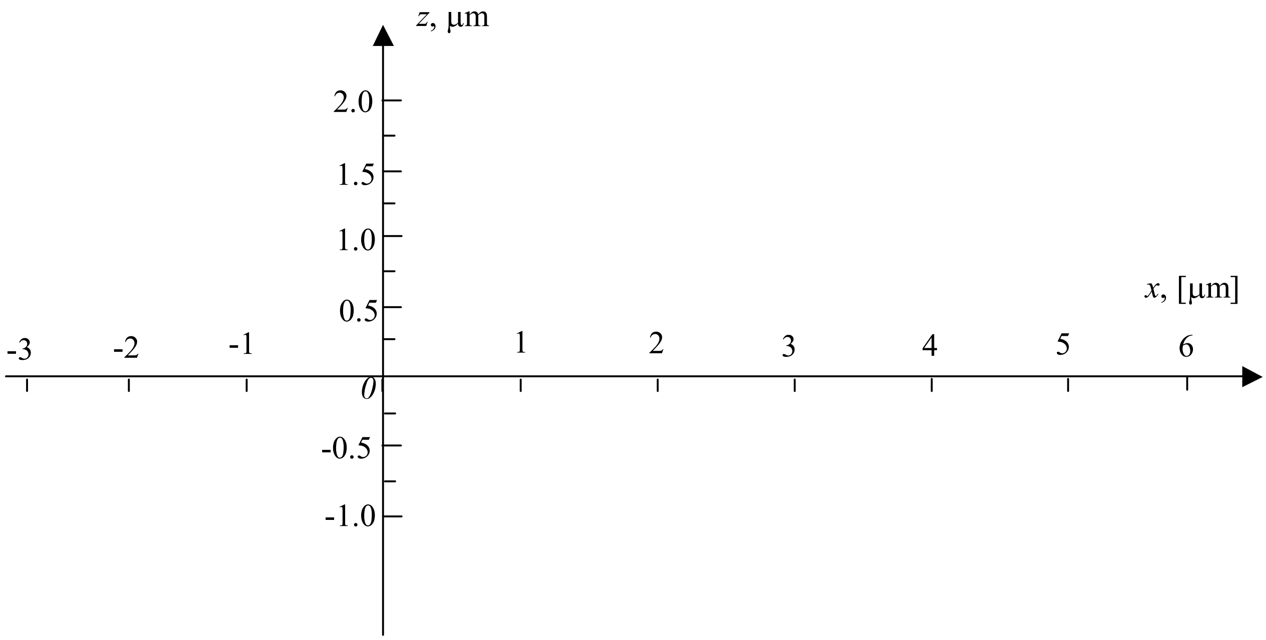


Process Sequence:

1. Starting material: boron-doped silicon, concentration 5 x 10^{15} cm^{-3}
2. Deposit 0.25 μm CVD SiO_2 and pattern using the **Oxide Mask 1** (dark field)
3. Implant boron with dose Q_a = 5 x 10^{11} cm^{-2} and anneal to a depth of 0.35 μm.
4. Etch off all oxide using a hydrofluoric acid wet etch.
5. Deposit 0.25 μm of CVD SiO_2 and pattern using the **Oxide Mask 2** (dark field).
6. Implant phosphorus with dose Q_d = 5 x 10^{11} cm^{-2} and anneal, after which the phosphorus layer's junction depth is 0.25 μm and the boron implant depth increases to 0.5 μm.
7. Deposit 0.5 μm of CVD SiO_2 and pattern using the **Contact Mask** (dark field).
8. Deposit 0.5 μm of aluminum and pattern using the **Metal Mask** (clear field).

Given: mobilities for this problem are μ_n = 1000 $cm^2/(Vs)$ and μ_p = 400 $cm^2/(Vs)$. Count the "dogbone" contact areas as 0.65 square each in finding the resistance.

(a) [5 pts.] Sketch the cross section ***A-A'*** on the graph below **after step 8**. Identify all layers clearly.

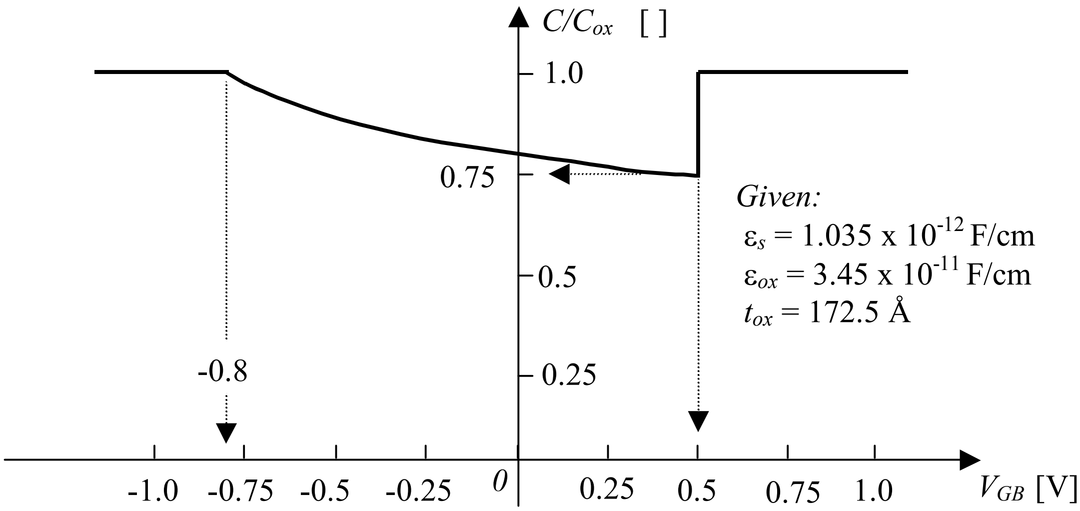


(b) [4 pts.] What is the sheet resistance $R_{\square 1}$ of Region 1 (see the layout) in Ω/□?

(c) [4 pts.] What is the sheet resistance $R_{\square 2}$ of Region 2 (see the layout) in Ω/□?

(c) [4 pts.] What is the resistance $R_{1\text{-}2}$ between terminals 1 and 2 in Ω? Make judicious approximations to find the effective width of the resistor. If you couldn't solve parts (c) and (d), use $R_{\square 1}$ = 200 Ω and $R_{\square 2}$ = 175 Ω in this part. (Note that these are incorrect answers to (c) and (d).

2. MOS Capacitor [17 pts.]



Given:
$\varepsilon_s = 1.035 \times 10^{-12}$ F/cm
$\varepsilon_{ox} = 3.45 \times 10^{-11}$ F/cm
$t_{ox} = 172.5$ Å

(a) [3 pts.] What is the numerical value of the flatband voltage V_{FB} of this MOS capacitor?

(b) [3 pts.] What is the numerical value of the threshold voltage V_{Tn} of this MOS capacitor?

(c) [3 pts.] The area of the MOS capacitor is 15 μm X 15 μm. What is the capacitance (units: fF) when $V_{GB} = 0.75$ V?

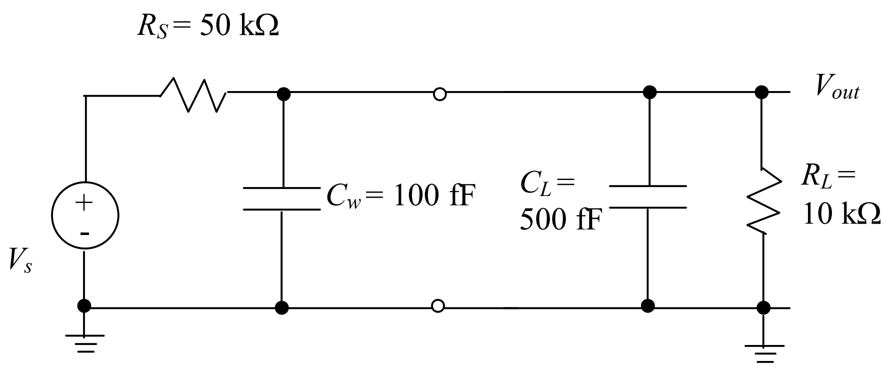
(d) [4 pts.] What is the numerical value of the inversion charge Q_N (units: Coulombs) for this 15 μm X 15 μm MOS capacitor when $V_{GB} = 1$ V?

(e) [4 pts.] If the gate-bulk voltage is

$$v_{GB}(t) = V_{GB} + v_{gb}(t) = -0.5V + 10mV\cos(2\pi \cdot 100x10^6\, t),$$

what is the current $i_{gb}(t)$? The units for the current should be nA (10^{-9} A).

3. Phasor Analysis [16 points]



(a) [4 pts.] Find the transfer function

$$H(j\omega) = V_{out} / V_s$$

for the above circuit. There is no need to substitute numerical values for the components.

(b) [4 pts.] Plot the magnitude of $H(j\omega)$ in dB, using the asymptotic (straight-line) approximations. You will need to substitute the numerical values.

(c) [4 pts.] Plot the phase of $H(j\omega)$ in degrees, using the asymptotic (straight-line) approximations. You will need to substitute the numerical values.

(d) [4 pts.] The source voltage is the cosine function $v_s(t) = 25mV\cos[2\pi(25MHz)t]$. Using your result from part (a), find the output voltage $v_{out}(t)$. If you couldn't solve part (a), you can assume that the transfer function is 0.5 at low frequency and that the –3 dB frequency is 50 MHz (not correct answers for (a), of course).