CE Frequency Response

- The "exact" analysis is worked out on pp. 639-641 of H&S.

$$\frac{V_{out}}{V_s} = \frac{-g_m\left(\frac{r_\pi}{r_\pi + R_S}\right)(r_o \| r_{oc} \| R_L)(1 - j\omega/\omega_z)}{(1 + j\omega/\omega_{p1})(1 + j\omega/\omega_{p2})}$$

The low-frequency voltage gain (loaded) is $-g_m\left(\frac{r_\pi}{r_\pi + R_S}\right)(r_o \| r_{oc} \| R_L)$

The zero is higher than the transition frequency $\omega_T = g_m/(C_\pi + C_\mu)$

The first (lowest frequency) pole is (approximately)

$$\omega_{p1} = \{(R_S \| r_\pi)[C_\pi + (1 + g_m R_{out}')C_\mu] + R_{out}' C_\mu\}^{-1}$$

where $R_{out}' = r_o \| r_{oc} \| R_L$

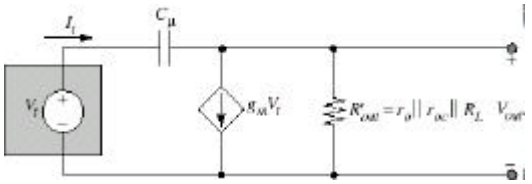
The second pole is (approximately)

$$\omega_{p2} = \frac{(R_S \| r_\pi)(R_{out}')}{(R_S \| r_\pi)[C_\pi + (1 + g_m R_{out}')C_\mu] + R_{out}' C_\mu}$$

- Brute force analysis is not particularly helpful for gaining insight into the frequency response ...

The Miller Approximation

- Therefore, we consider the effect of C_μ on the input node only



neglect the feedforward current I_μ in comparison with $g_m V_\pi$ ... a good approximation

$I_t = (V_t - V_o) / Z_\mu$

$V_o = - g_m V_t R_L / (R_L + R_{out}') = A_{vC\mu} V_t$

where $A_{vC\mu}$ is the low frequency voltage gain across C_μ

$I_t = V_t (1 - A_v) / Z_\mu$

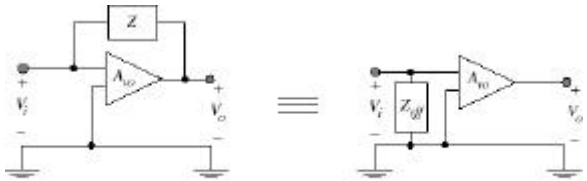
$Z_{eff} = V_t / I_t = Z_\mu / (1 - A_v)$

$$Z_{eff} = \frac{1}{j\omega C_\mu}\left(\frac{1}{1 - A_{vC_\mu}}\right) = \frac{1}{j\omega(C_\mu(1 - A_{vC_\mu}))} = \frac{1}{j\omega C_M}$$

$C_M = (1 - A_{vC_\mu})C_\mu$ is the **Miller capacitor**

Generalized Miller Approximation

- An impedance Z connected across an amplifier with voltage gain A_{vZ} can be replaced by an impedance to ground ... multiplied by $(1 - A_{vZ})$



$$Z_{eff} = Z/(1 - A_{VO})$$

- Common-emitter and common-source:

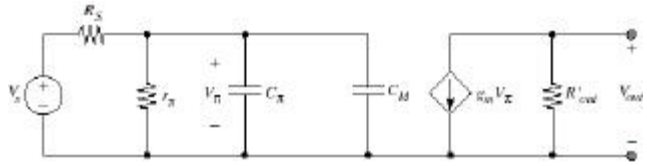
  A_{vZ} = large and negative for C_μ or C_{gd} --> capacitance at the input is **magnified**

- Common-collector and common-drain:

  $A_{vZ} \approx 1$ --> capacitance at the input due to C_π or C_{gs} is greatly **reduced**

Voltage Gain vs. Frequency for CE Amplifier Using the Miller Approximation

- The Miller capacitance is lumped together with C_π, which results in a single-pole low-pass RC filter at the input



$$C_M = C_\mu(1 + g_m R'_{out})$$

- Transfer function has one pole and no zero after Miller approximation:

$$\omega_{3dB}^{-1} = (r_\pi || R_S)(C_\pi + C_M)$$

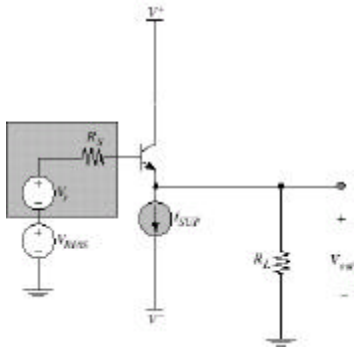
$$\omega_{3dB}^{-1} = (r_\pi || R_S)[C_\pi + (1 + g_m r_o || r_{oc} || R_L)C_\mu]$$

$\omega_{3dB}^{-1} \approx \omega_1^{-1}$ from the exact analysis (final term $R_{out}{}'C_\mu$ is missing)

- The break frequency is reduced by the Miller effect ... which results in a large Miller capacitor at the input.

Common Collector Frequency Response

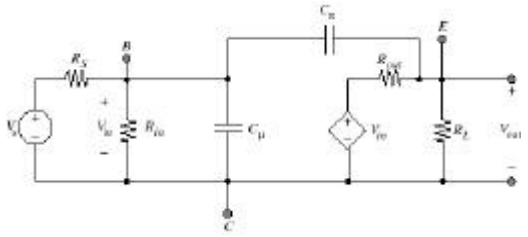
Basic approach: two-port model from Chapter 8, "decorated" with device capacitances



The DC output voltage V_{OUT} is selected to be 0 V, so that the output voltage is just the small-signal voltage v_{out} (phasor representation V_{out})

Common-Collector Frequency Response

- Voltage buffer two-port model has input at base and output at emitter:



Note carefully where the capacitances are connected!

"Millerize" the base-emitter capacitor: gain across it is $A_{v\pi} = \dfrac{R_L}{R_L + R_{out}}$

$$C_M = C_\pi(1 - A_{v\pi}) = C_\pi\left(1 - \left(\frac{R_L}{R_L + R_{out}}\right)\right) = C_\pi\left(\frac{R_{out}}{R_L + R_{out}}\right)$$

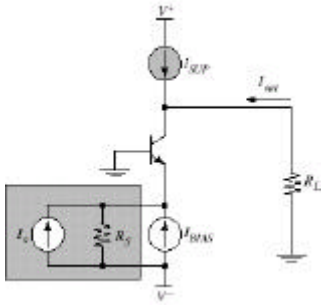
The break frequency of the common-collector is:

$$\omega_{-3dB} = \frac{1}{(R_S \| R_{in})(C_\mu + C_M)}$$

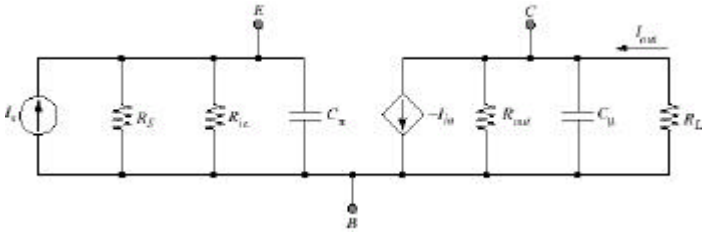
can approach the transition frequency for small source resistances

Common-Base Frequency Response

Similar approach: start with two-port and add capacitors ....



Two-port model:



Common-Base Frequency Response

- Poles are separate (no coupling between input and output)

$$\omega_{p,\,in} = \frac{1}{(R_S \| R_{in}) C_\pi}$$

$$\omega_{p,\,out} = \frac{1}{(R_{out} \| R_L) C_\mu}$$

- The input pole is beyond the transition frequency, due to the low value of $R_{in} = 1/g_m$
- The output pole is a function of R_L since the output resistance is so large. For small load resistances, the output pole can approach the transition frequency

Summary of single-stage amplifiers:

CE/CS: Miller effect decreases the bandwidth severely

CC/CD: wideband

CB/CG: wideband

Multistage Amplifiers

- Single-stage transistor amplifiers are inadequate for meeting most design requirements for **any** of the four amplifier types (voltage, current, transconductance, and transresistance.)
- Therefore, we use more than one amplifying stage. The challenge is to gain insight into when to use which of the **9** single stages that are available in a modern BiCMOS process:

  Bipolar Junction Transistor: CE, CB, CC -- in npn and pnp* versions

  MOSFET: CS, CG, CD -- in n-channel and p-channel versions

  * in most BiCMOS technologies, only the npn BJT is available
- How to design multi-stage amplifiers that satisfy the required performance goals?

*** Two fundamental requirements:**

1. Impedance matching:

output resistance of stage n, $R_{out,\,n}$ and input resistance of stage $n + 1$, $R_{in,\,(n+1)}$, must be *in the proper ratio*

$R_{in,\,(n+1)} / R_{out,\,n} \dashrightarrow \infty$ or $R_{in,\,(n+1)} / R_{out,\,n} \dashrightarrow 0$

to avoid degrading the overall gain parameter for the amplifier

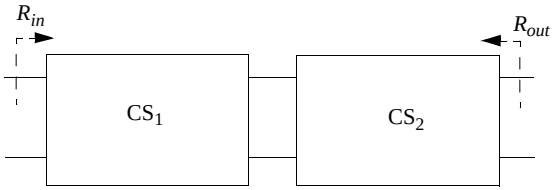
2. DC coupling:

we will directly connect stages: effect on DC signal levels must be considered, too

Example 1: Cascaded Voltage Amplifier

- Want R_{in} --> infinity, R_{out} --> 0, with high voltage gain.

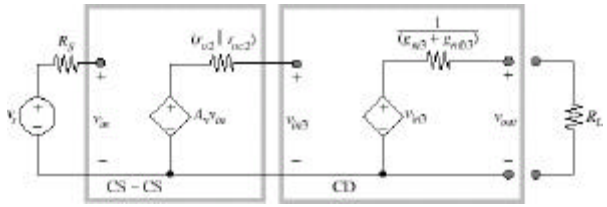
  Try CS as first stage, followed by CS to get more gain ... use 2-port models



- solve for overall voltage gain ... higher, but $R_{out} = R_{out2}$ which is too large

Three-Stage Voltage Amplifier

- Fix output resistance problem by adding a common drain stage (voltage buffer)

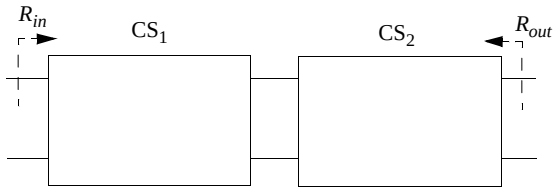


- Output resistance is not that low ... few kΩ for a typical MOSFET and bias --> could pay an area penalty by making (W/L) very large to fix.

Cascaded Transconductance Amplifier

- input resistance should be high; output resistance should also be high

  initial idea: use CS stages (they are “natural” transconductance amps)

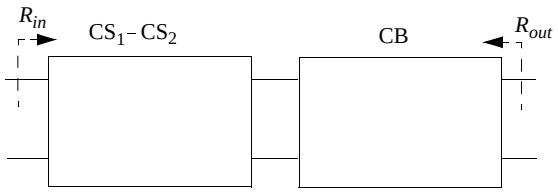


- Overall $G_m = - g_{m1} (r_{o1} \| r_{oc1}) g_{m2} = A_{v1} g_{m2}$ ... can be very large

  BUT, output resistance is only moderately large ... need to increase it

Improved Transconductance Amplifier

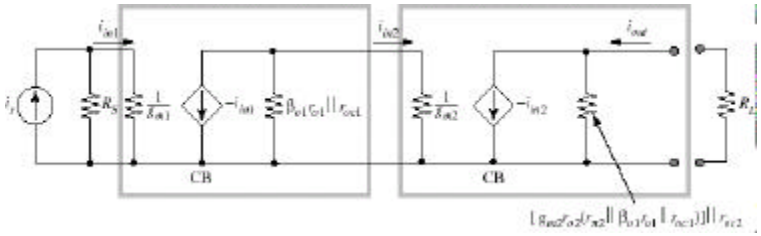
- Output resistance: boost using CB or CG stage



- high-source resistance current sources are needed to avoid having r_{oc3} limit the resistance

Two-Stage Current Buffers

- since one CB stage boosted the output resistance substantially, why not add another one ...



- The base-emitter resistance of the 2nd stage BJT is $r_{\pi 2}$ which is much less than the 2nd stage source resistance = 1st stage output resistance

$$R_{S2} = R_{out1} = \beta_{o1} r_{o1} \| r_{oc1}$$

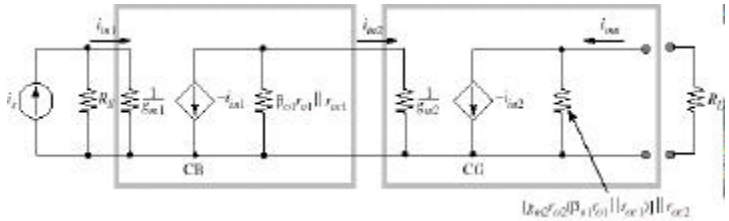
- Therefore, the output resistance expression reduces to

$$R_{out} \approx g_{m2} r_{o2} r_{\pi 2} \| r_{oc2} = \beta_{o2} r_{o2} \| r_{oc2}$$

... no improvement over a single CB stage

Improved Two-Stage Current Buffer: CB/CG

- The addition of a common-gate stage results in further increases in the output resistance, making the current buffer closer to an ideal current source at the output port



- The product of transconductance and output resistance $g_{m2}\, r_{o2}$ can be on the order of 500 - 900 for a MOSFET --> R_{out} is increased by over two orders of magnitude ... practical limit ... on the order of 100 MΩ

  Of course, the current supply for the CG stage has to have at least the same order of magnitude of output resistance in order for it not to limit R_{out}.

- General "resistance matching" ... try not to lose much in doing a current divider or a voltage divider. Which of these is appropriate depends on whether the signal is current or voltage at the port.