Microelectronic Devices and Circuits- EECS105

Second Midterm Exam

Wendesday, November 17, 1999

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Your Name:	OFFICIAL	SOLUTIONS	
	(last)	(first)	
Your Signature:	h Enaws		

- 1. Print and sign your name on this page before you start.
- 2. You are allowed two, 8.5"x11" handwritten sheets with formulas. No books or notes!
 - 3. Do everything on this exam, and make your methods as clear as possible.

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TOTAL	59.1 /1	00	AVERAGE	(67 students)
Problem 3	/	35		
Problem 2	/	35		
Problem 1	/	30		

Problem 1 of 3 Answer each question briefly and clearly. (30 points)

Explain briefly why BJT performance depends so much on the diffusivity of minority carriers (5pts)

It is the diffusion of minority carriers that brians them to the reverse-blosed collector junction that mohes the transistor work

How does the small signal output resistance of a BJT depend on its size (emitter-to-base junction area), when V_{BE} is held constant? (5pts)

$$I_{c} = I_{s} \cdot e^{V_{BE}/V_{th}} \qquad 2_{o} = \frac{V_{A}}{I_{c}}$$

$$I_{c} \text{ is proportional to } I_{s}, \text{ and } I_{s} \text{ is proportional to } A_{E}.$$

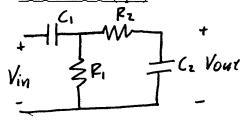
$$S_{o} : A_{E} \uparrow => I_{s} \uparrow => I_{c} \uparrow => 7_{o} \downarrow$$

Why is it desirable for $V_{BS} = 0V$ in MOS Common Gate applications? (5pts)

What happens to the overall (loaded) |Av| when Ic increases in a CE amplifier? (Assume that R_L is initially equal to ro, Rs<<r π and r_{oc} = infinity)(5 pts)

$$\begin{aligned}
Q_{m} &= \frac{I_{c}}{Vth} & Z_{o} &= \frac{V_{A}}{I_{c}} \\
|A_{V}| &= Q_{m} \left(\frac{7_{o}}{I_{RL}} \right) &= \frac{I_{c}}{Vth} & \frac{7_{o} R_{L}}{2_{o} + R_{L}} &= \frac{V_{A}}{Vth} & \frac{V_{A}}{I_{c}} + R_{L} \\
&=> |A_{V}| &= \frac{V_{A}}{Vth} & \frac{P_{L}}{V_{A}} & \text{so, if Jcf then } |A_{o}| \uparrow \uparrow.
\end{aligned}$$

How many poles and how many zeros does this circuit have? What is its function, assuming that $R_1C_1 << R_2C_2$? (5pts)



this is a band pass silter, with one jw F, C, mult.

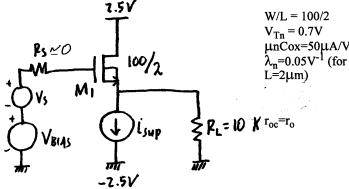
Fr. T Cz Vour or pole ar 1/F, Cz and one pole ar 1/F, C, (notice that you have two cascaded voltage dividers).

Assuming no loading"

Problem 2 of 3 (35 points)

For each of the following questions, make sure that you show the expressions <u>before</u> you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

You are given the following nmos common drain amplifier.



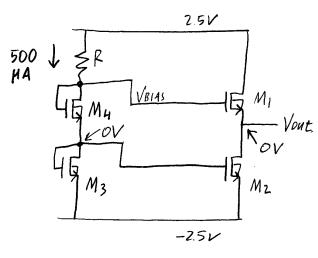
a) Assume V_{bs} =0v, and find V_{bias} so that I_{sup} = 500 μ A. (10pts) 4nd $\sqrt{000}$ = 0V

$$V_{GS} = \sqrt{\frac{2I_{DS}}{\frac{W}{L}}} + V_{TN} = 1.332V$$
. Since $V_S = 0V$, the $V_{GS} = V_{BAS} \neq 1.332V$

b) Calculate the overall (loaded) voltage gain, with V_{bs} =0V. (10pts)

The unloaded voltage gain is
$$A_{V} = \frac{g_{M}}{1 + g_{M}} = 0.969$$
 $g_{M} = \sqrt{2 \frac{W}{L} \mu_{M} cox I_{D}} = 1.58 \text{m/s}$
 $\frac{1}{20 || 7_{0L}} + g_{M}} = 0.969$
 $\frac{1}{20 || 7_{0L}} + g_{M}} = 6139$
 $\frac{1}{20 || 7_{0L}} + g_{M}} = 6139$
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c) Size the biasing transistors and resistor in order to get the proper V_{bias} and proper supply current (10pts)



$$V_{B145} = 1.332 V. \Rightarrow P = \frac{2.5V - 1.332 V}{500 \mu A} = \frac{23369}{500 \mu A}$$

My must have 1.332 of Vos =>
$$\frac{M_1}{N_0 V_{out}} = \frac{2 \text{IDS} / 4 \text{nCox}}{\sqrt{\frac{W}{L} / 4 \text{nCox}}} + \sqrt{4 \text{n}} = 1.332 = \sqrt{\frac{W}{L} / \frac{2}{4}} = \frac{2 \text{IDS} / 4 \text{nCox}}{\sqrt{1.332 - V_{tn}}} = \frac{100}{2}$$
M2

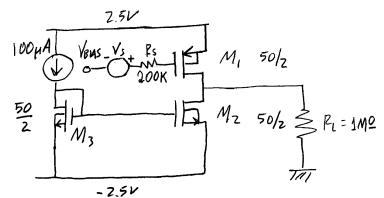
$$\sqrt{\frac{2I_{DS}}{(\frac{W}{L})_{3}^{2}}} + V_{7n} = 7.5 \Rightarrow \left(\frac{W}{L}\right)_{3}^{2} = \frac{2I_{DS}/\mu n(ox)}{(2.5 - V_{7n})^{2}} = 6.17$$

$$\alpha \ell so, \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = 6.17. = \frac{12.30}{2}$$

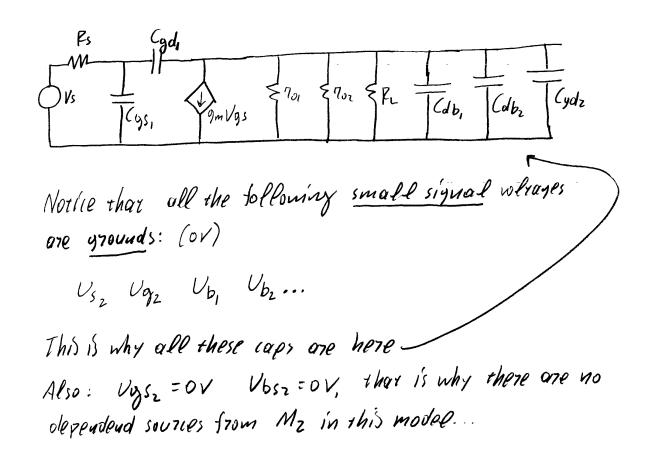
Problem 3 of 3 (35 points)

For each of the following questions, make sure that you show the expressions <u>before</u> you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

You are given the following p-channel common-source amplifier.



a) Draw the small signal model of the amplifier. Make sure that you include the entire small signal model of transistor M_1 , along with all the relevant capacitances, including r_{o2} , C_{db2} and C_{gd2} from the current sink transisotr M_2 . (10 points)



b) Apply the Miller approximation (ignore all capacitances when calculating the Miller gain), and derive a symbolic expression for the complete transfer function (hint: this function has two poles and no zeros) (7 points).

$$C_{M} = (1+|A_{V}|) C_{GD_{1}} \qquad A_{V} = -9m \left(\frac{201}{202} \|P_{L}\right)$$

$$V_{OUT} = -V_{S} \cdot \frac{\frac{1}{|W(C_{9S_{1}} + C_{M})|}}{|P_{S} + \frac{1}{|W(C_{9S_{1}} + C_{M})|}} \cdot 9m \left(\frac{201}{202} \|P_{L}\| \frac{1}{|W(C_{9S_{1}} + C_{M})|}\right) = 7$$

$$\frac{V_{OUT}}{V_{S}} = -\frac{9m}{[1 + \frac{1}{|W(C_{9S_{1}} + C_{M})|}]} \cdot \frac{201}{[1 + \frac{1}{|W(C_{9S_{1}} + C_{M})]}} \cdot \frac{201}{[1 + \frac{1}{|W(C_{9S_{1}} + C_{M})]}} \cdot \frac{201}{[1 + \frac{1}{|W(C_{9S_{1}} + C_{M})]}]} \cdot \frac{201}{[1 + \frac{1}{|W(C_{9S_{1}} + C_{M})]}} \cdot \frac{201}{[1 + \frac{1}{|W(C_{9S_{1}} + C_{M})]}]} \cdot \frac{201}{[1 + \frac{1}{|W(C_{9S_{1}} + C_{M})]}} \cdot \frac{201}{[1 + \frac{1}{|W(C_{9S_{1}} + C_{M})}} \cdot \frac{201}{[1 + \frac{1}{|W(C$$

c) Calculate dc gain and the values of the two poles, given that C_{gs1} =78fF, C_{gd1} =25fF, C_{gd2} =25fF, C_{db1} =90fF, C_{db2} =30fF (8 points)

$$dc \ gain = -9m \left(\frac{701}{701} \right) = -32.214$$

$$9m = \sqrt{2 \frac{W}{L}} \ln(ox_{10}) = 0.354mS$$

$$701 = (10.10)^{-1} = 200K = 702$$

$$pole 1 \ (dominanz) = \frac{1}{P_{S} \left((9s, + (M_{1})) - 25.5Mnad/ec} \right)}$$

$$\frac{25.5F \times (1+32214) = 8055F}{(701)(701)(R_{L}) \cdot ((dh_{1}t)(dh_{1}t)(gdz))}$$

d) Draw the Bode plot for amplitude and phase of the gain of this amplifier (10 points).

