Lumped Approximation

The dimension of the physical circuit is **small** enough so that electromagnetic waves propagate across the circuit "almost" instantaneously.

Rule of Thumb

Lumped Approximation is valid if

$$d \ll c \bullet \Delta t$$

$d =$ largest dimension of the physical circuit

$\Delta t =$ smallest signal response time of interest

$=$ 1/max. frequency of interest

$c = 3 \times 10^8\ m/\mathrm{sec}$

Example : hi-fi set

max. frequency of interest = 25 Khz

$\therefore$ Lumped approximation holds if

$$d \ll 3(10^8)m/s \bullet \frac{1}{25(10^3)} = 12\ Km$$

$$\approx 7.5 miles$$

$\therefore$ Even if the circuit is spread across a football stadium, it satisfies the lumped approximation.

Consequences of Lumped Approximation

1. Electrical behavior does not depend on the physical size, shape, and orientation. Only the physical interconnections are relevant. Hence each device can be lumped into a point, as in classical mechanics.
2. Voltages and currents at any terminal of the physical circuit are well defined.

Basic Circuit Theory

3 Postulates :

1. Lumped Approximation
2. Kirchhoff Current Law (KCL)
3. Kirchhoff Voltage Law (KVL)

Circuit Theory is applicable if, and only if, the above 3 postulates are satisfied.

Current is a “through” variable

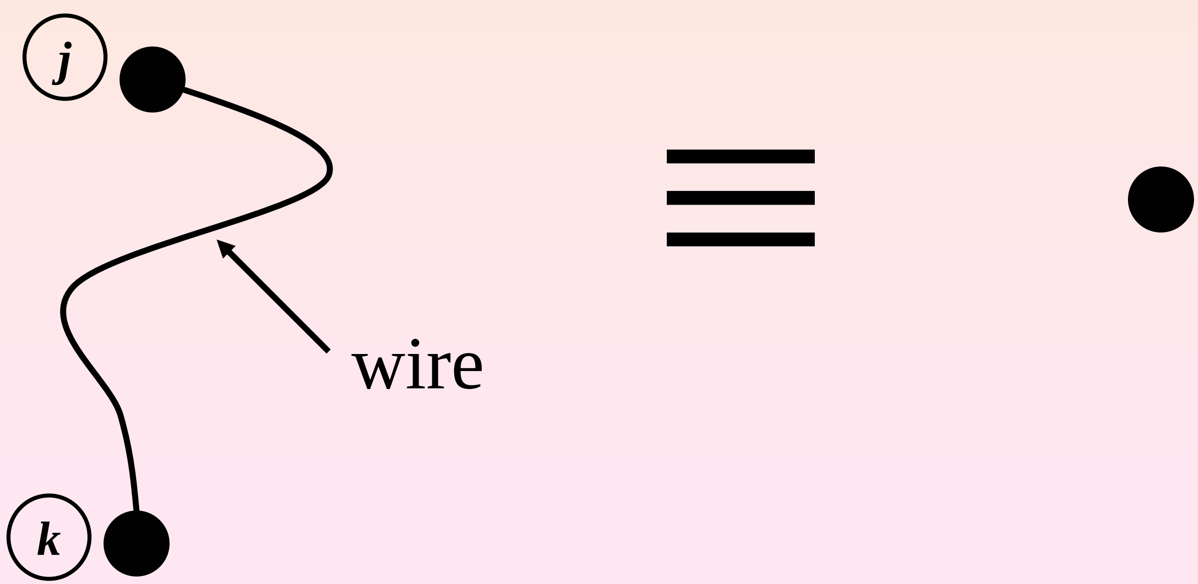
Current is always measured by inserting an **Ammeter** **through** 1 point of a device terminal or wire.

Assumption 1

1. All conducting wires are perfect conductors (zero resistance).
2. All circuit interconnections are perfect.

Consequence

Two terminals joined by a wire is equivalent to a single terminal.



Quantum Mechanical Tunneling makes perfect contacts

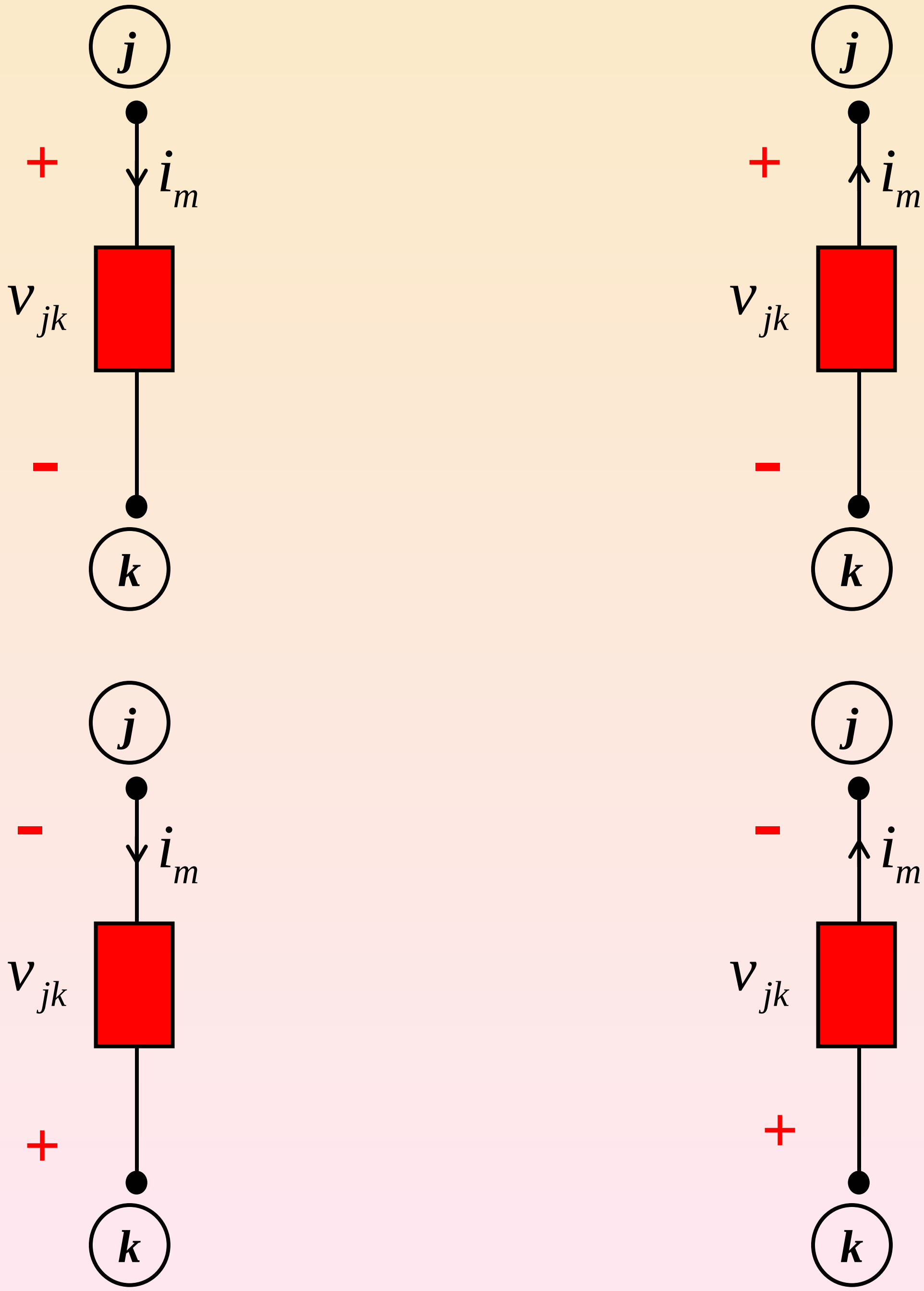
Since the 2 metal prongs of an electrical **plug** has a thin oxide layer (perfect insulator) on all sides, the perfect contact established when it is plugged into a **socket** is due to a quantum-mechanical phenomenon called **tunneling**.

Reference Current Direction and Voltage Polarity

Since the current $i(t)$ entering an electrical terminal k and the voltage $v_{jk}(t)$ across a pair of terminals j and k in a typical electrical circuit can assume a ***positive*** value at one instant of time, and a ***negative*** value at another instant of time, it is necessary to assign **(arbitrarily) a current reference** direction for each terminal current, and an **a pair of voltage polarity reference**, across every pair of terminals.

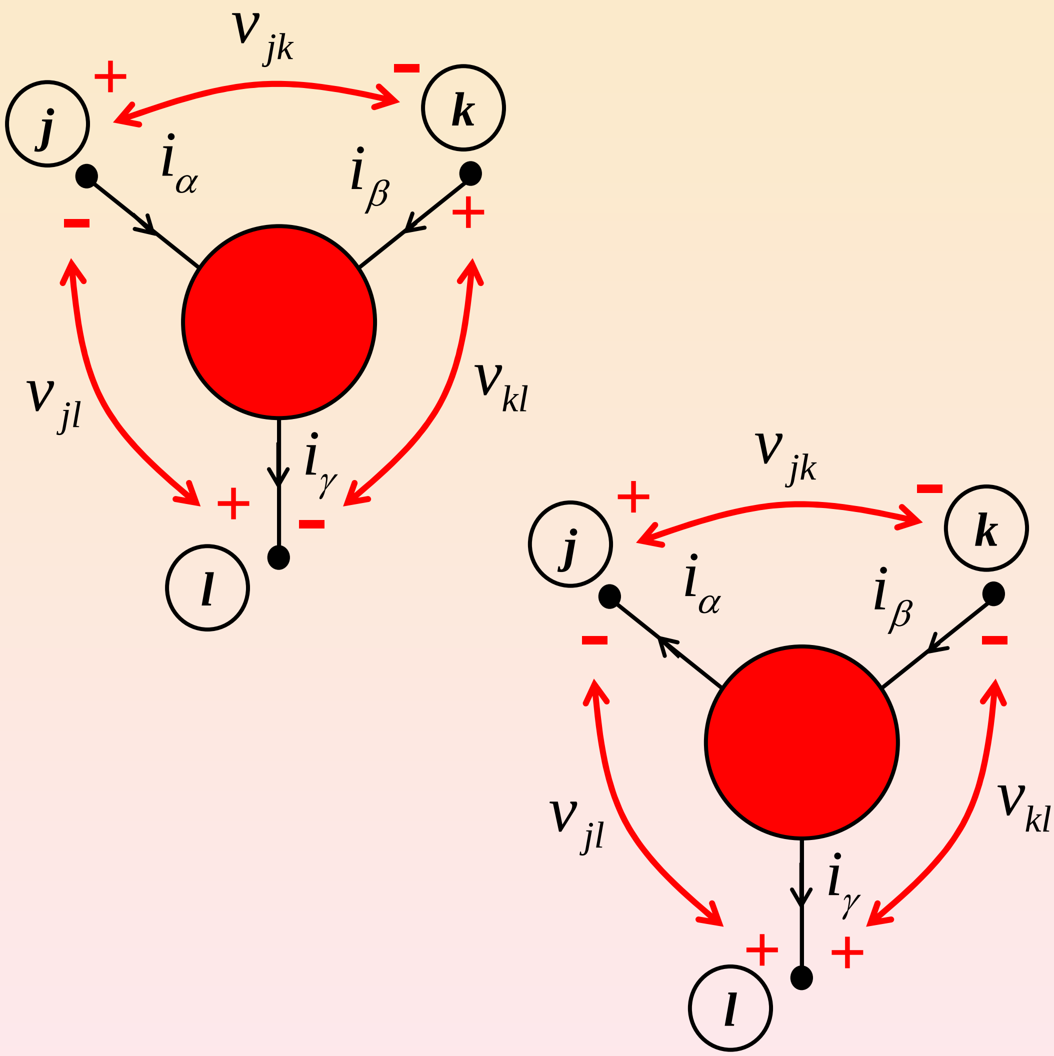
If the calculated current (resp., voltage) at some instant of time turns out or be a **negative** number, it simply means that the **actual** current (resp., voltage) is **opposite** in direction (resp., polarity) to the arbitrarily assigned reference at that instant of time.

4 possible reference assignments for a 2-terminal device



Reference current direction and reference voltage polarity can be arbitrarily assigned.

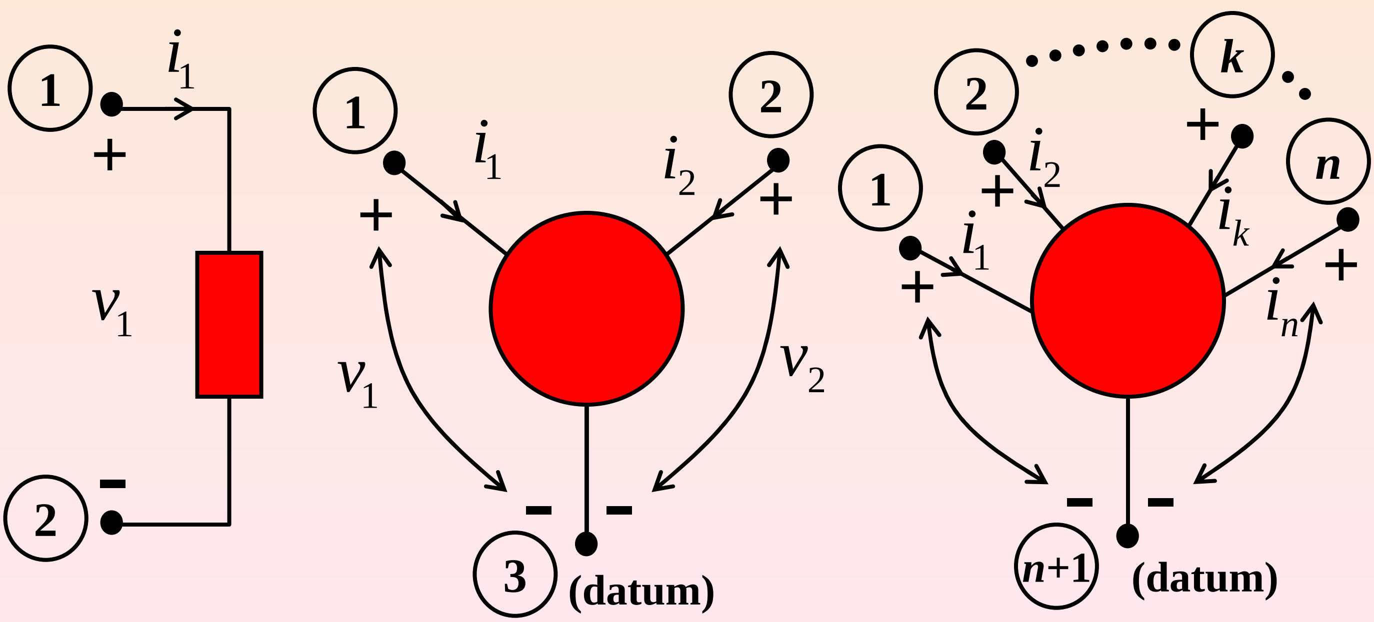
2 Among many possible reference assignments



Note: When two terminals whose voltage polarity is being assigned are far apart, we often draw a double-headed arrow to identify the associated pair of terminals.

Associated Reference Convention

Although the reference current direction and the voltage polarity can be arbitrarily assigned, for pedagogical reasons, we will agree on the following **associated reference convention**:



2-terminal device

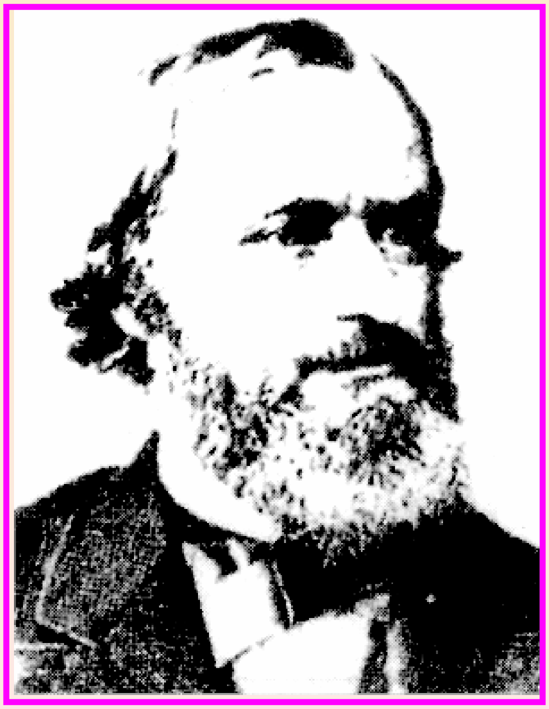
3-terminal device

(n+1)-terminal device

Current is assigned entering the positively referenced non-datum terminal.

Voltage is an “across” variable

Voltage is always measured by connecting a **voltmeter** **across** 2 device terminals or nodes.

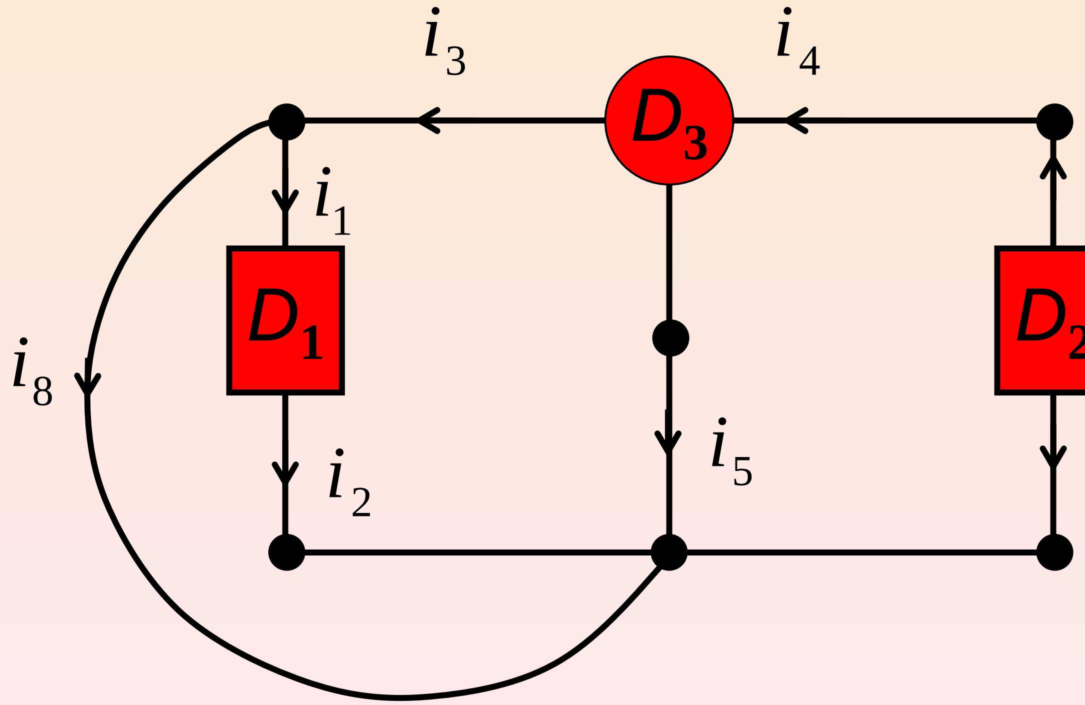


Gustav Robert Kirchhoff (1824-1887)

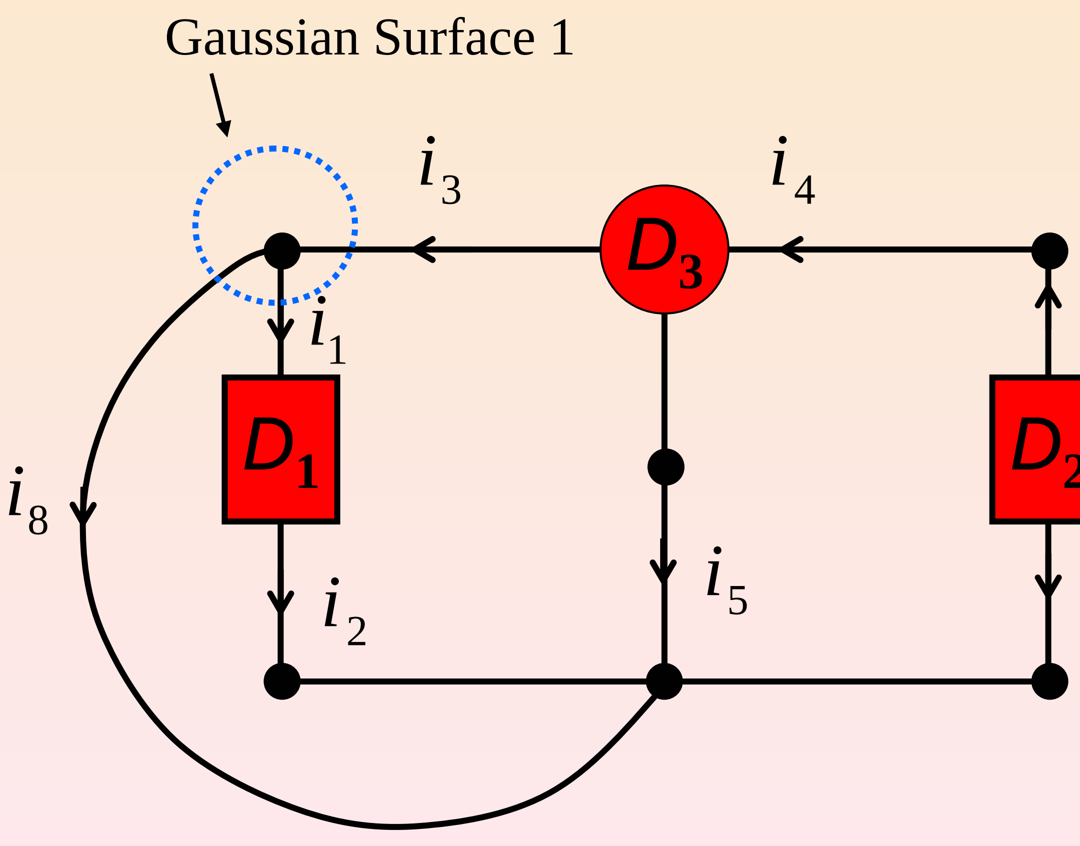
Gaussian Surface

Any **closed surface** that has an **inside** and an **outside** is called a **Gaussian surface**.

KCL



KCL



Gaussian Surface 1: $i_1 - i_3 + i_8 = 0$

Nodes

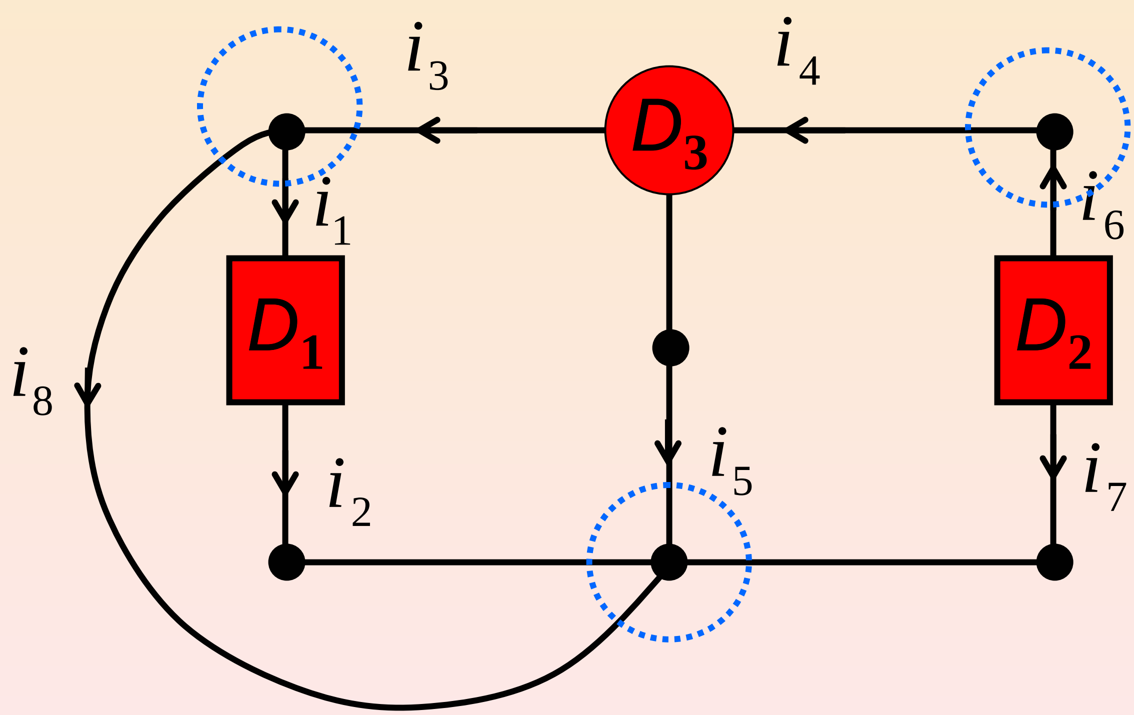
Definition

Any terminal (i.e., wires) attached to a device in a circuit where 2 or more terminals are soldered together is called a **node**.

Remarks:

1. We can always draw a sufficiently small sphere centered at each node of a circuit such that the sphere is pierced only by the currents entering the node.
2. A sphere is the simplest Gaussian surface.

KCL

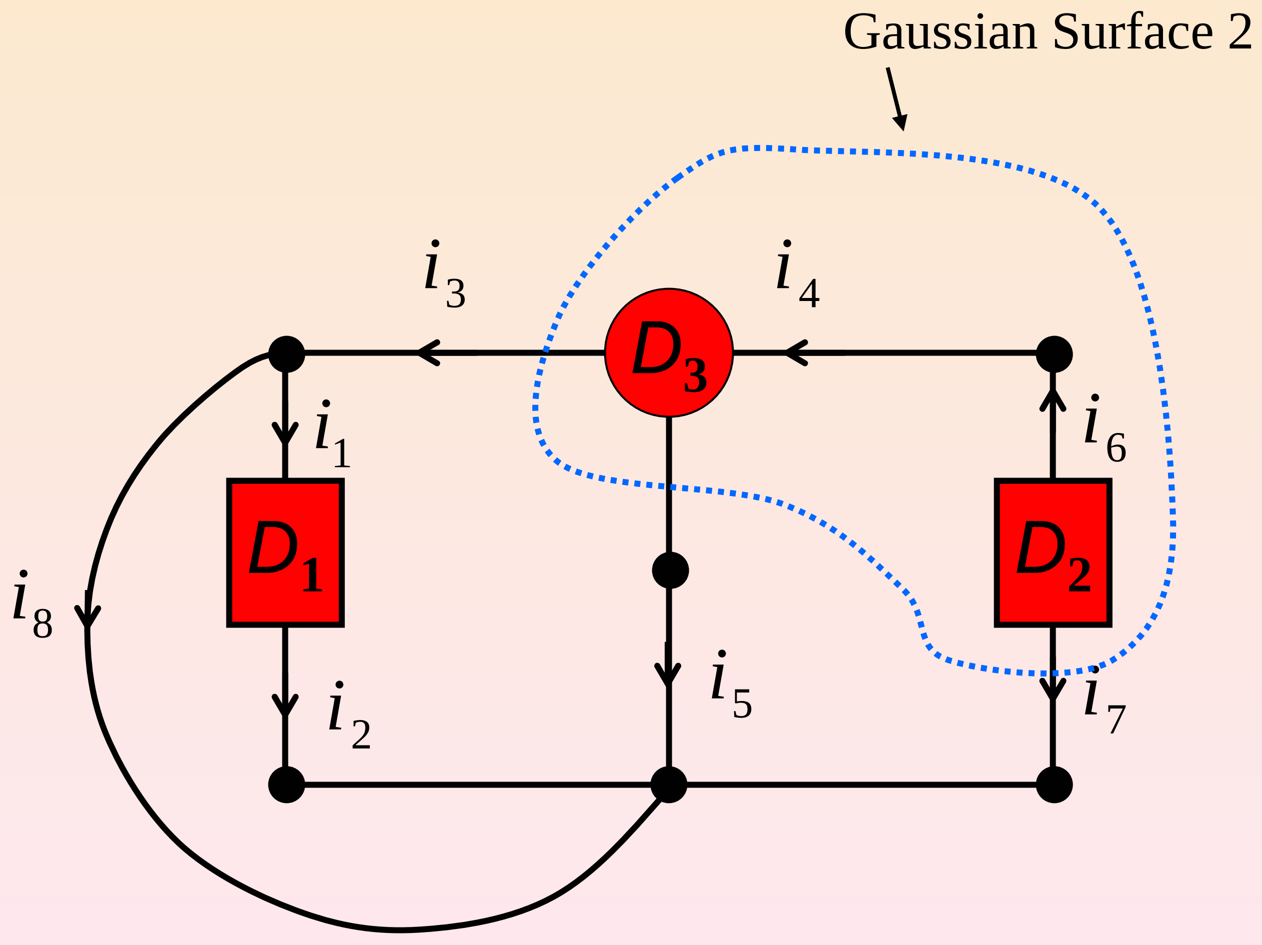


Applying KCL to a small Gaussian surface enclosing each node

$\Rightarrow$ **Corollary 1**

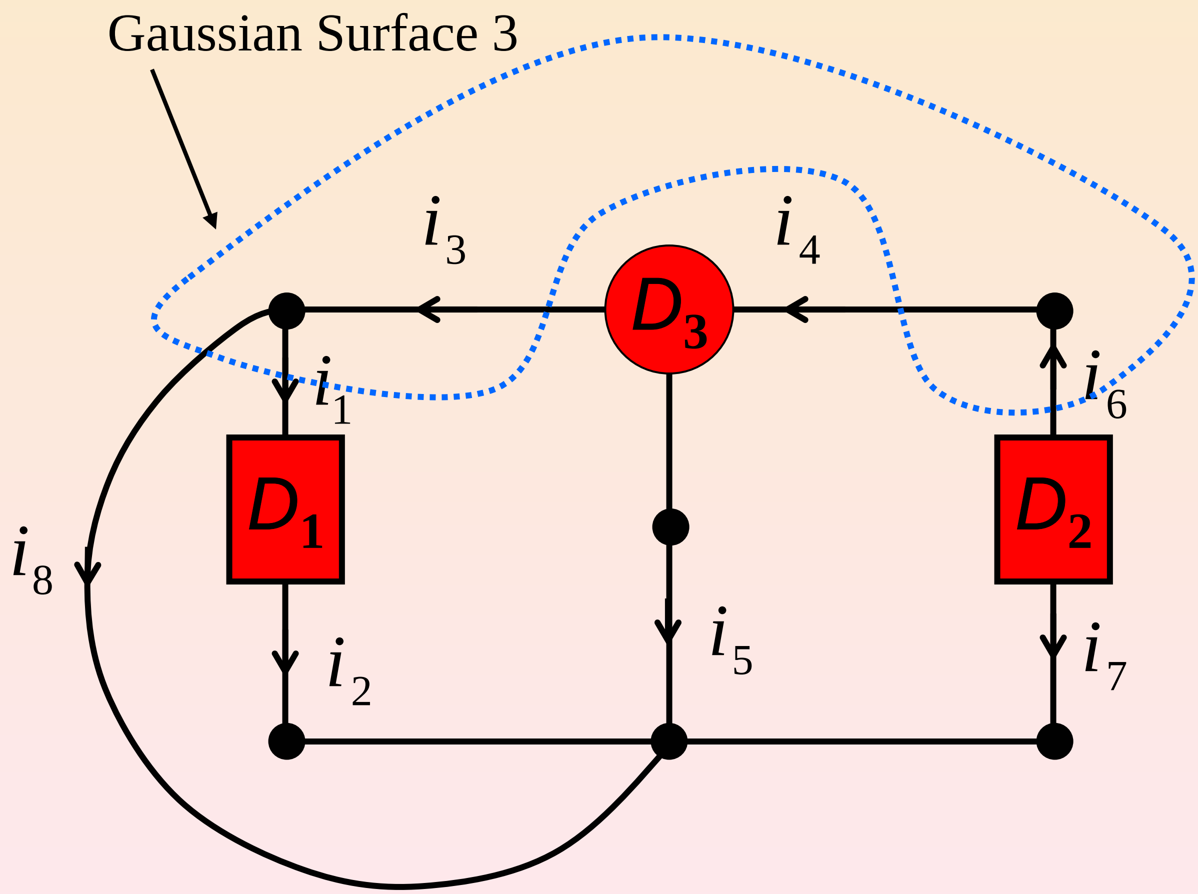
The algebraic sum of all currents leaving a **node** is zero.

KCL



Gaussian Surface 2: $i_3 + i_5 + i_7 = 0$

KCL



Gaussian Surface 3:

$$i_1 - i_3 + i_4 - i_6 + i_8 = 0$$

Cut set

Definition:

A subset of currents i_a, i_b …, i_m from a **physically connected** circuit forms a **cut set** **iff** the following 2 conditions are satisfied:

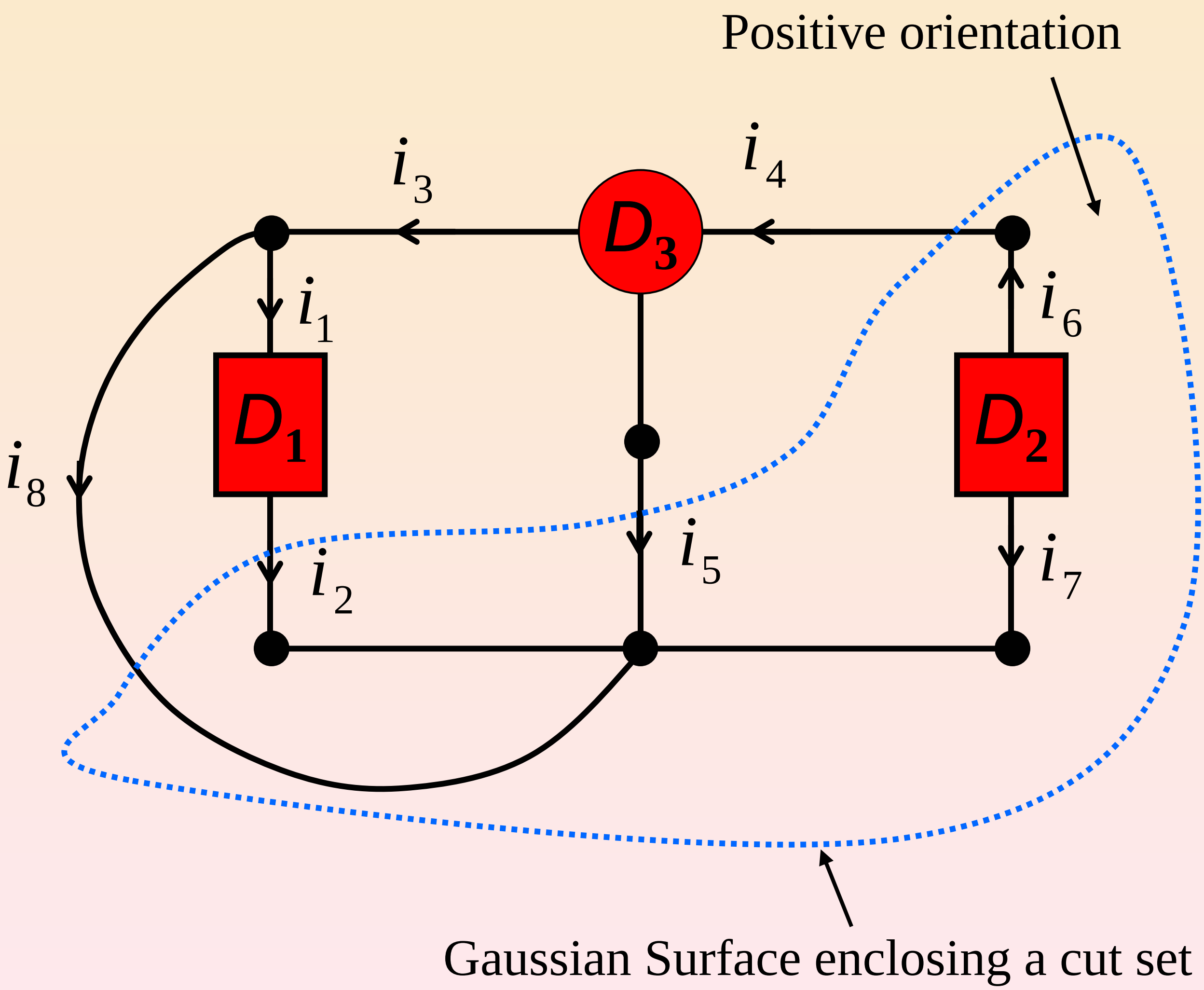
1. Cutting (say, with a plier) all "*m*" terminals (wires) would physically **disconnect** the circuit into 2 or more components.

2. Cutting only *m-1* terminals (wires) from (the subset of currents would **not** physically disconnect the circuit.

Remarks:

1. Given any cut set $\{i_a, i_b \ldots, i_m\}$, we can always draw a **Gaussian surface** pierced **only** by $\{i_a, i_b \ldots, i_m\}$.
2. Once a Gaussian surface is chosen, we define the direction of each current entering the surface to be the **positive** orientation of the cut set.
3. A cut set with an assumed **positive** orientation is said to be an **oriented** cut set.

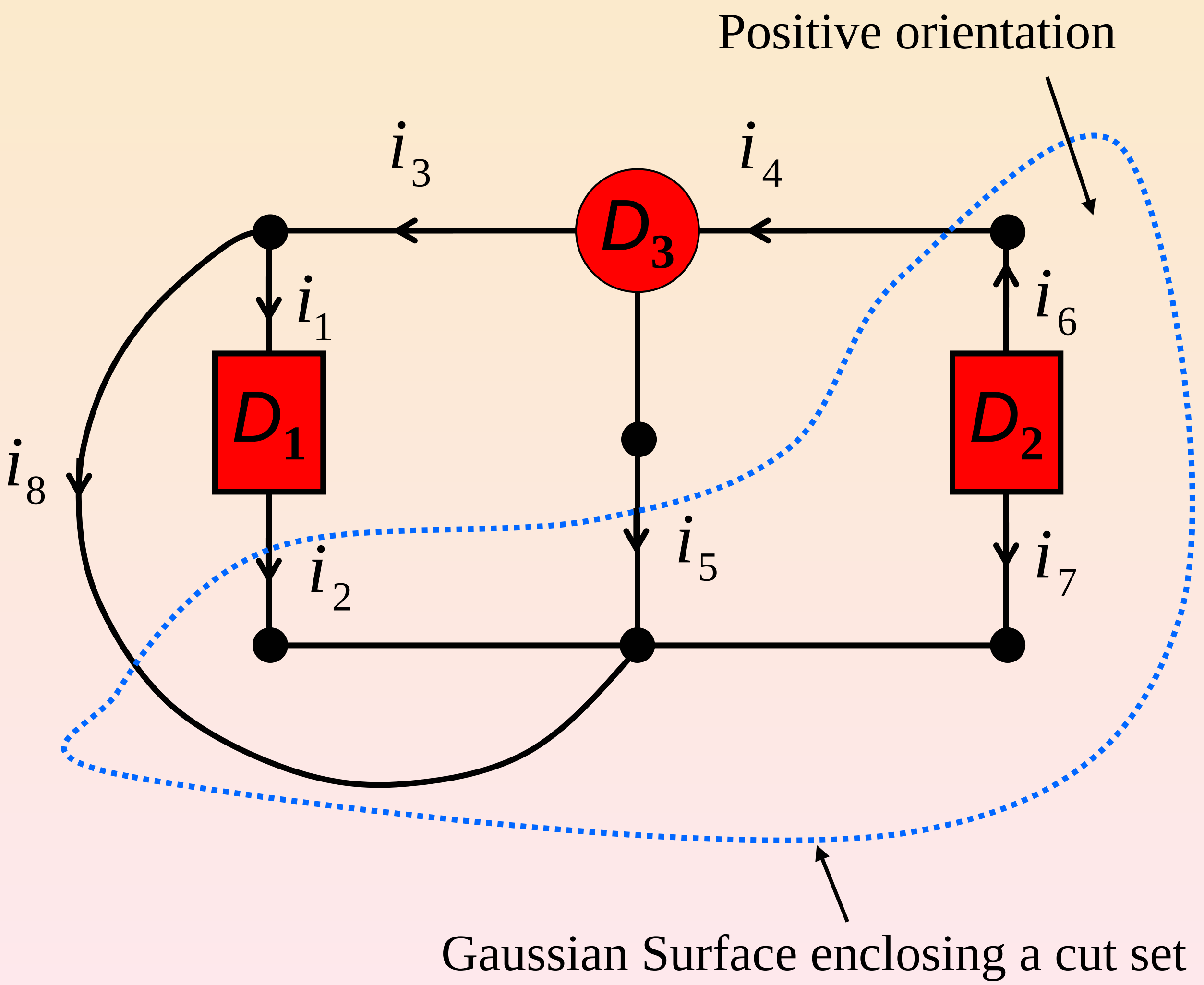
KCL



$\{i_2, i_4, i_5, i_8\}$ is a cut set because

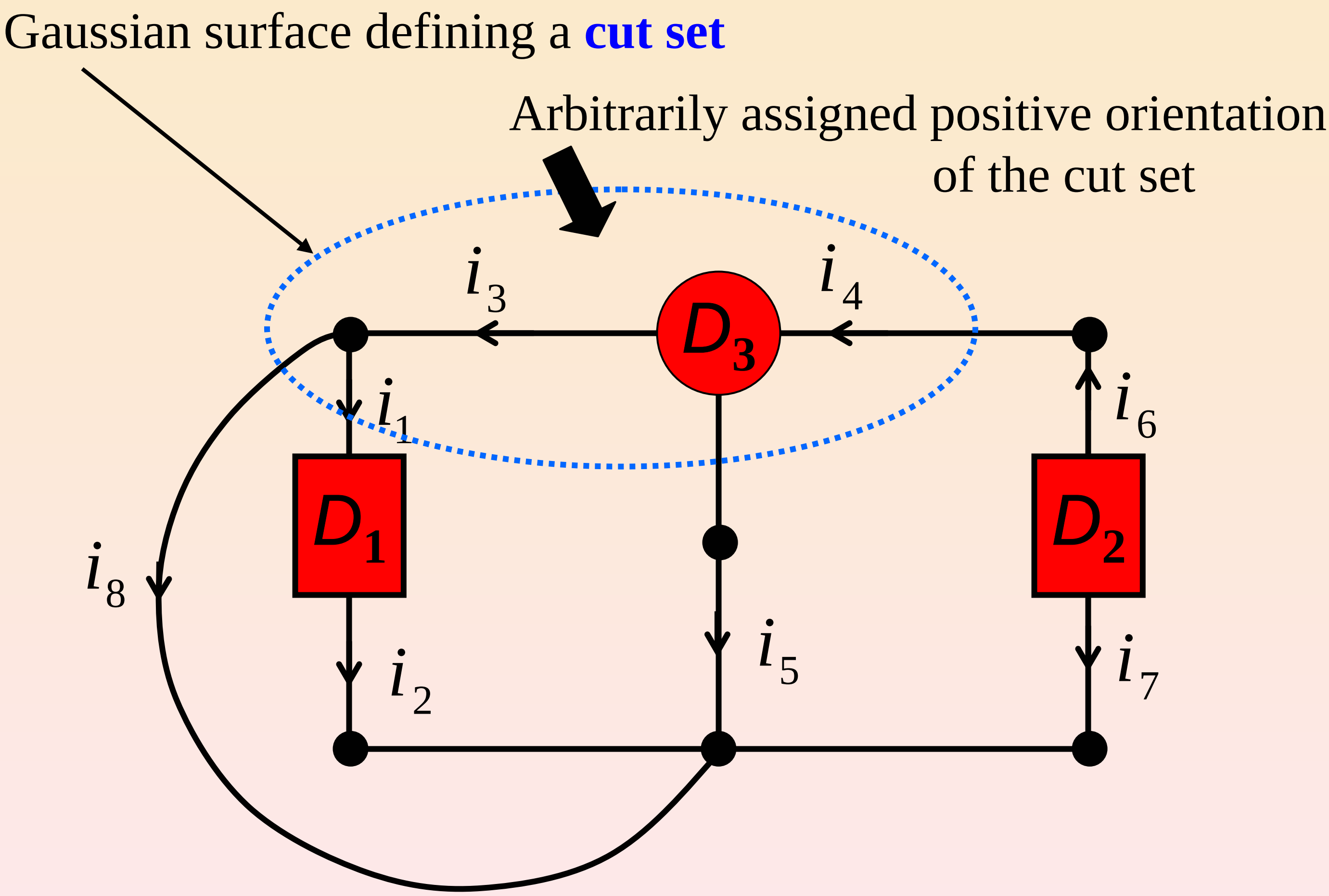
1. It cuts the circuit into 2 parts.
2. Any 3 out of 4 currents in the set will not cut the circuit.

KCL



$\{i_2, i_3, i_4, , i_5, i_8\}$ is not a cut set because the smaller subset $\{i_2, i_4, i_5, i_8\}$ can already cut the circuit into 2 parts.

KCL

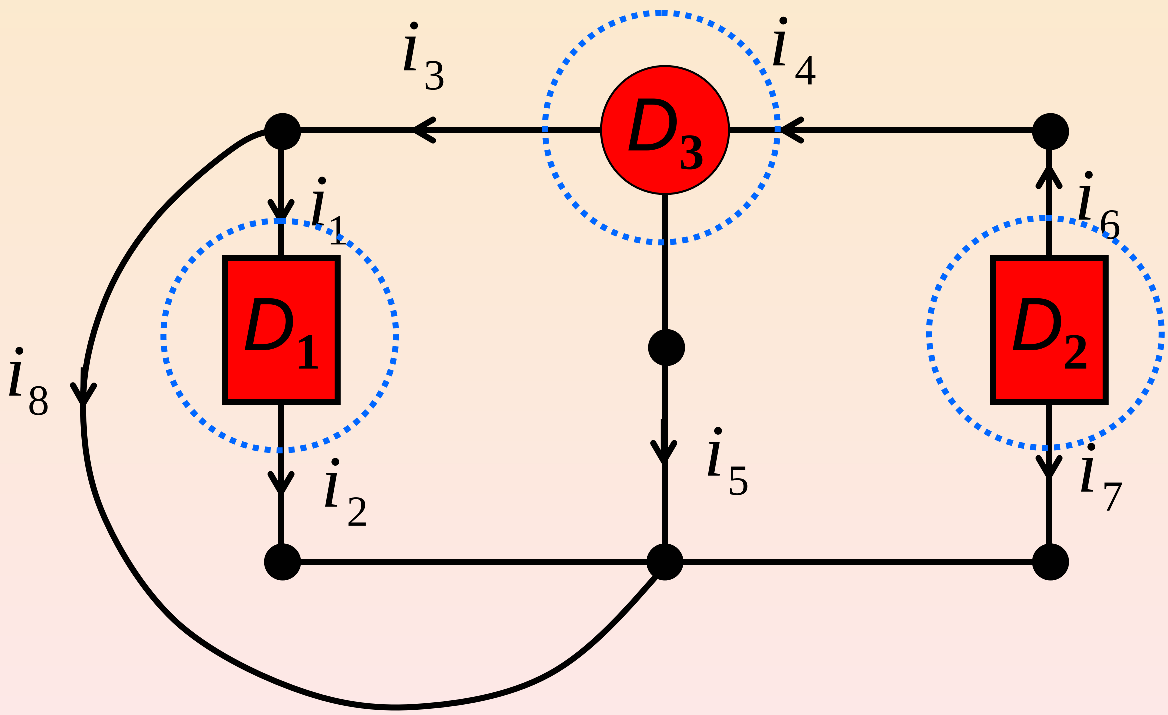


Applying KCL to a Gaussian surface associated with a cut set

$\Rightarrow$ **Corollary 2**

The algebraic sum of all currents in a **cut set** relative to its assigned positive orientation is zero.

KCL



Applying KCL to a Gaussian surface enclosing each device $\Rightarrow$

$$-i_1 + i_2 = 0$$

$$i_3 - i_4 + i_5 = 0$$

$$i_6 + i_7 = 0$$

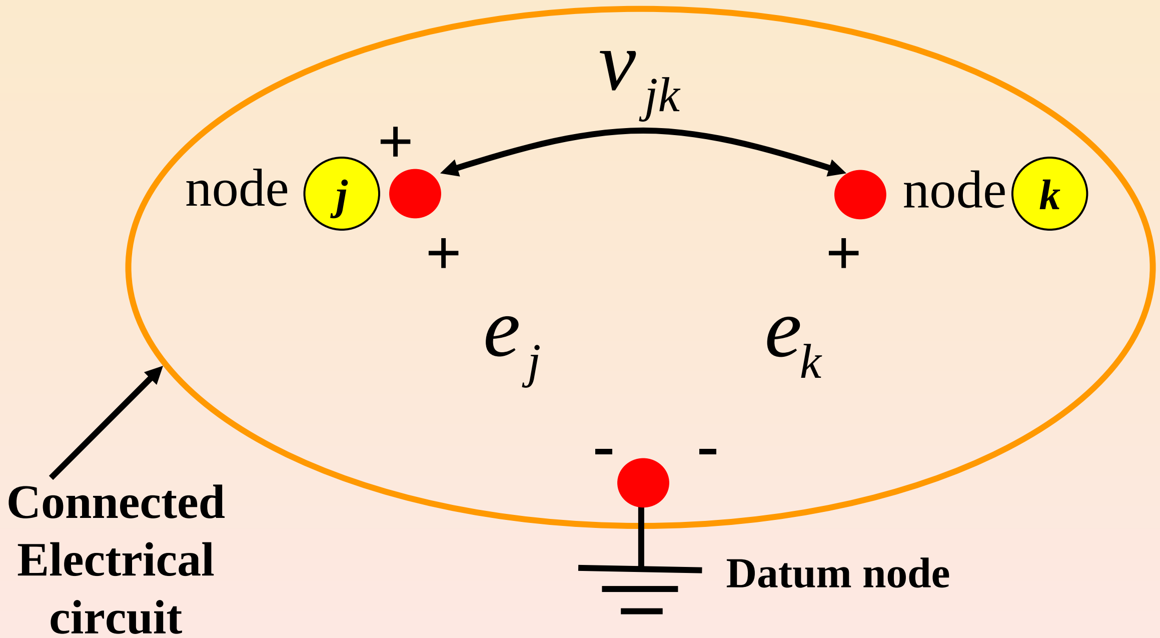
Node-to-datum and Branch voltages

In order for **work** to occur, the **test charge** has to be moved over some distance. So **voltage always involves two positions**, a starting point and an ending point.

To avoid ambiguity, we must always specify a voltage **across** 2 points in a circuit, called **nodes**, unless one of the 2 nodes is the circuit **ground** node, called the **datum node**. Such a voltage is called a ***node-to-datum*** voltage, and will always be denoted by e_j.

Any other voltage is called a **branch voltage**, and will be denoted by v_j.

Kirchhoff Voltage Law
KVL



The **voltage** $v_{jk}(t)$ between ***any*** 2 **nodes** j and k is equal to the difference between the 2 associated node-to-datum voltages e_j and e_k, for all times t.

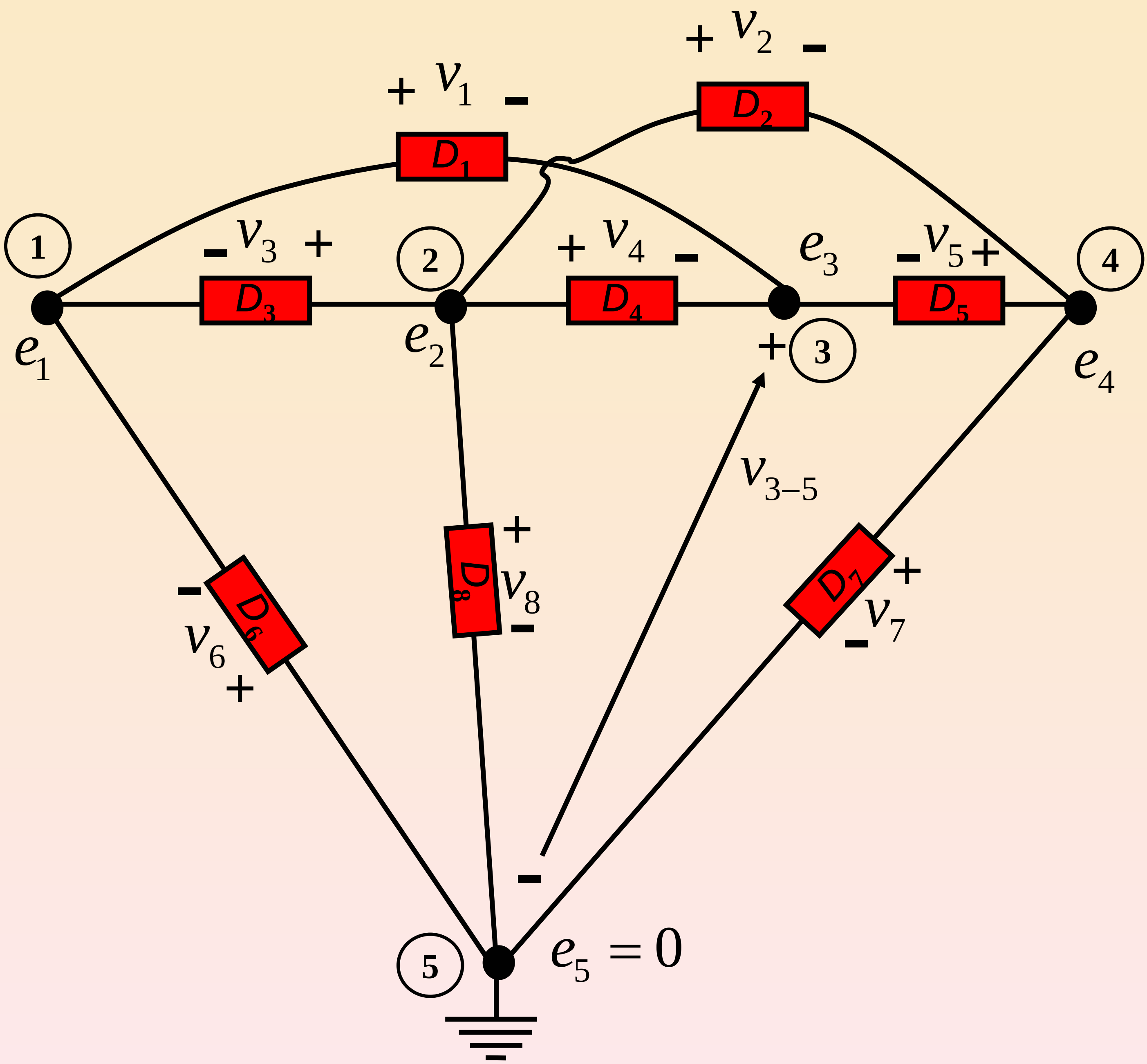
$$\boxed{v_{jk}(t) = e_j(t) - e_k(t)}$$

KVL

Corollary 1

(around **closed node sequences**)

Algebraic sum of **all voltages** around any **closed node sequence** in any connected circuit is equal to **zero** at all times t.



KVL $\Rightarrow$

$$v_1 = e_1 - e_3 \qquad v_5 = e_4 - e_3$$

$$v_2 = e_2 - e_4 \qquad v_6 = e_5 - e_1 = -e_1$$

$$v_3 = e_2 - e_1 \qquad v_7 = e_4 - e_5 = e_4$$

$$v_4 = e_2 - e_3 \qquad v_8 = e_2 - e_5 = e_2$$

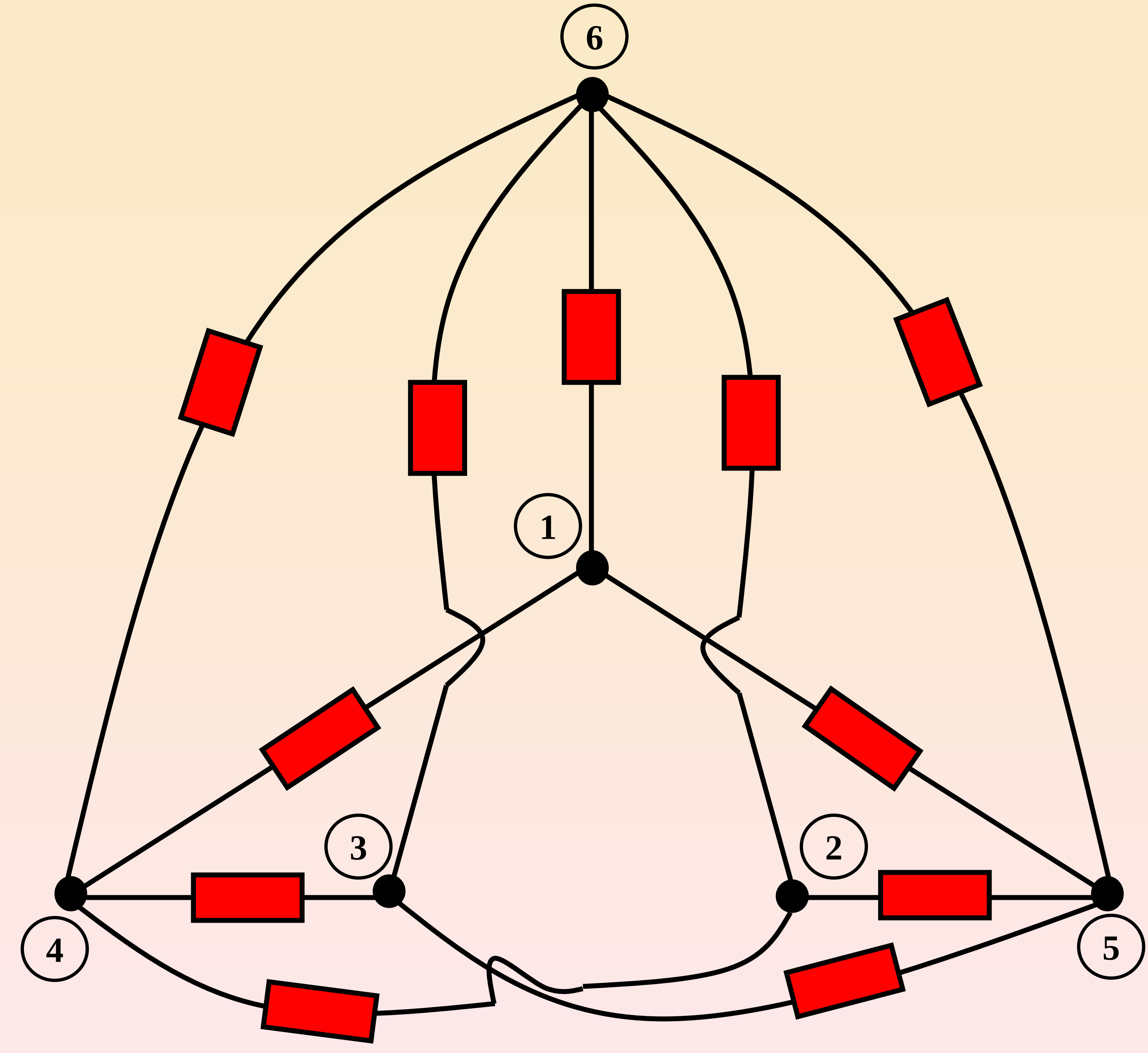
Consider Loop formed **by closed node sequence**

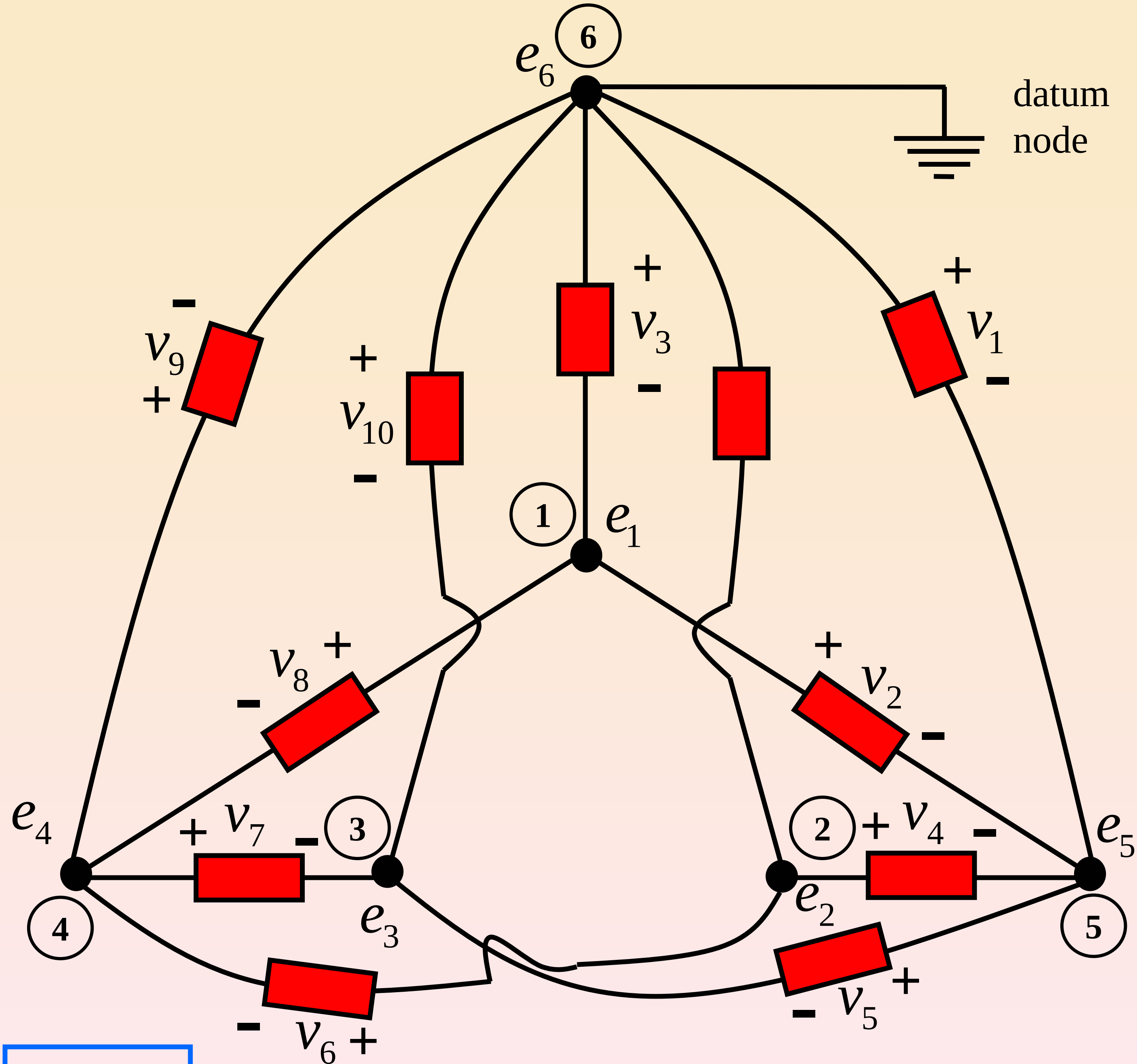
$$① \rightarrow ② \rightarrow ⑤ \rightarrow ① :$$

$$-v_3 + v_8 + v_6$$

$$= -(e_2 - e_1) + (e_2 - e_5) + (e_5 - e_1)$$

$$= 0$$


6
1
3
2
4
5

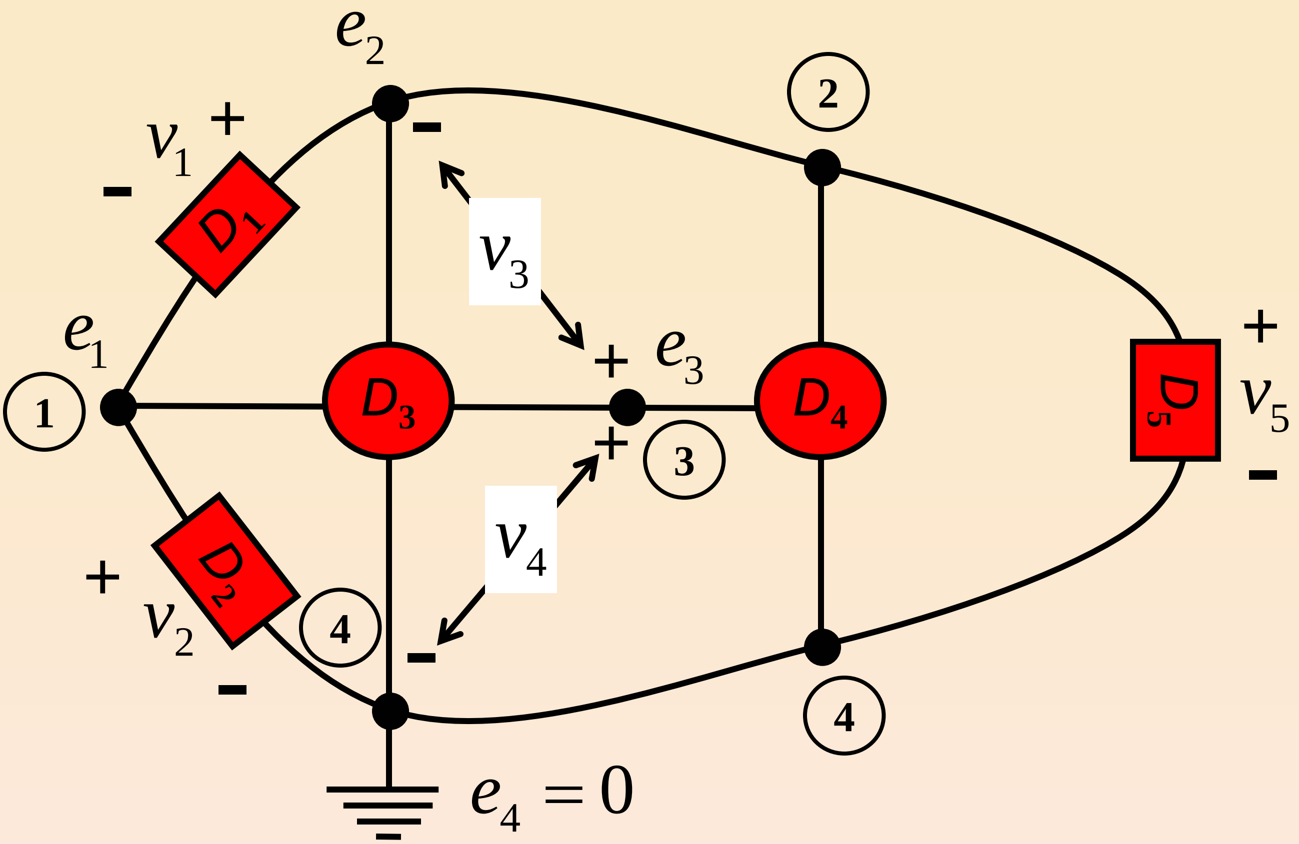


KVL

$$v_1 = e_6 - e_5 = -e_5, \quad v_4 = e_2 - e_5$$

$$v_2 = e_1 - e_5 \quad , \quad v_5 = e_5 - e_2$$

$$v_3 = e_6 - e_1 = -e_1, \quad v_6 = e_2 - e_4$$



$\boxed{\textbf{KVL}}$

$$v_1 = e_2 - e_1$$

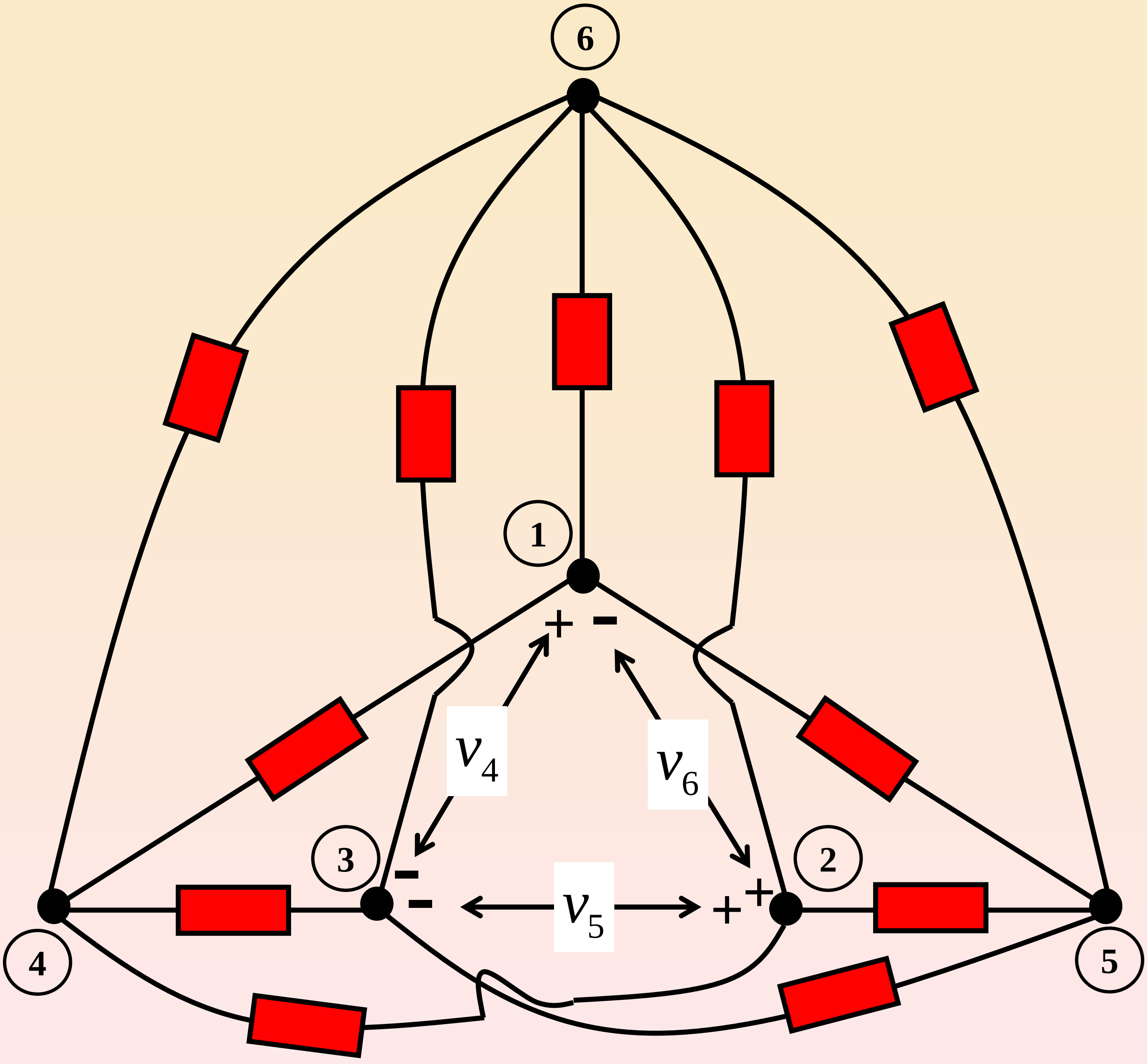
$$v_2 = e_1 - e_4 = e_1$$

$$v_3 = e_3 - e_2$$

$$v_4 = e_3 - e_4 = e_3$$

$$= \overbrace{(e_2 - e_1)}^{v_1} + \overbrace{(e_1 - e_4)}^{v_2} - \overbrace{(e_3 - e_4)}^{v_4} + \overbrace{(e_3 - e_2)}^{v_3}$$

$$= 0$$



KVL around closed node sequence

1 → 3 → 2 → 1 :

$$v_4 - v_5 + v_6 = 0$$

Loop

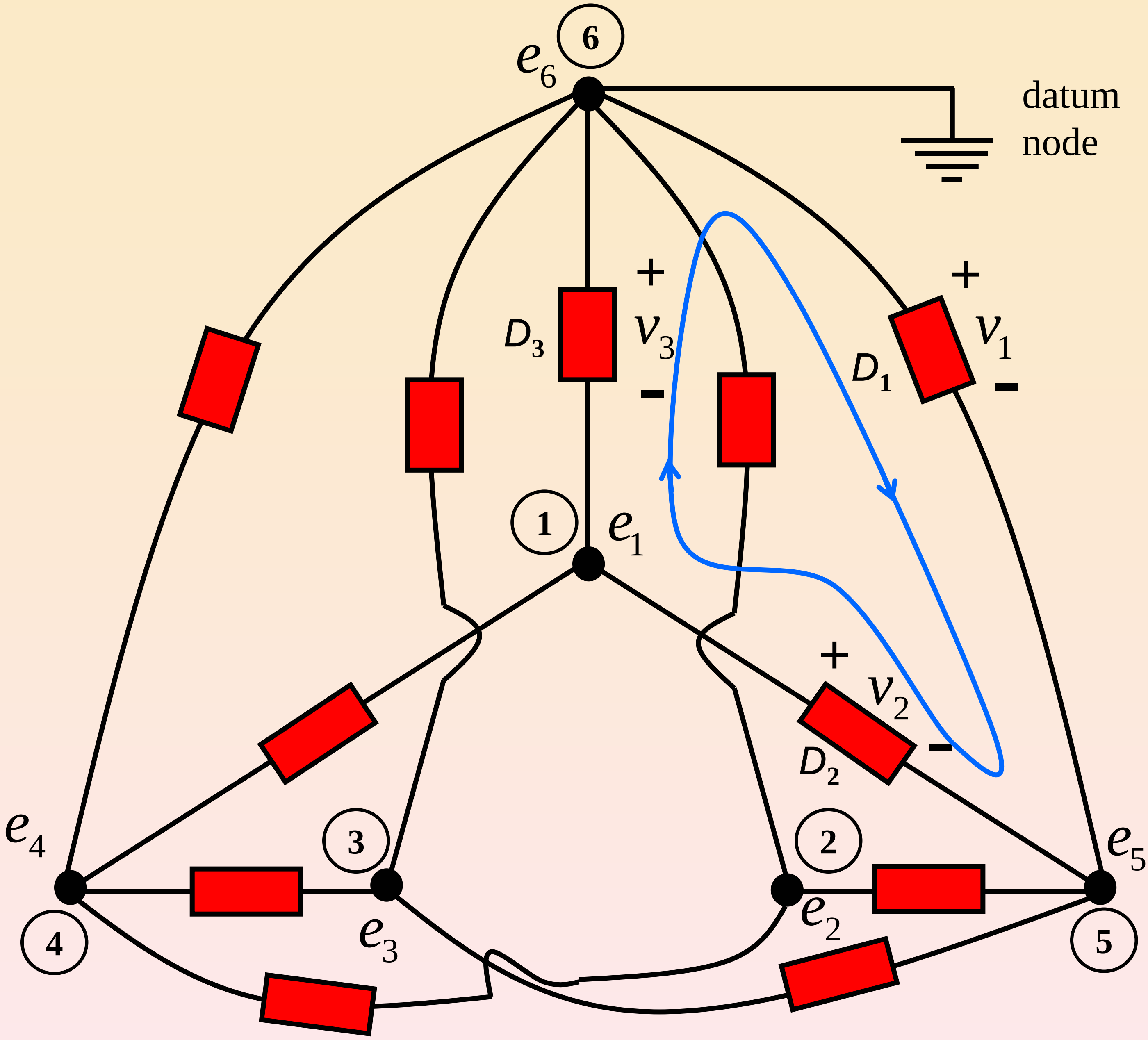
Definition

A closed node sequence $(n_a, n_b, \ldots, n_m)$ is called a **loop** iff, there is a 2-terminal circuit element connecting each consecutive pair of nodes (n_k, n_{k+1}), where n_k is any node in the sequence.

KVL

Corollary 2 **(around loops)**

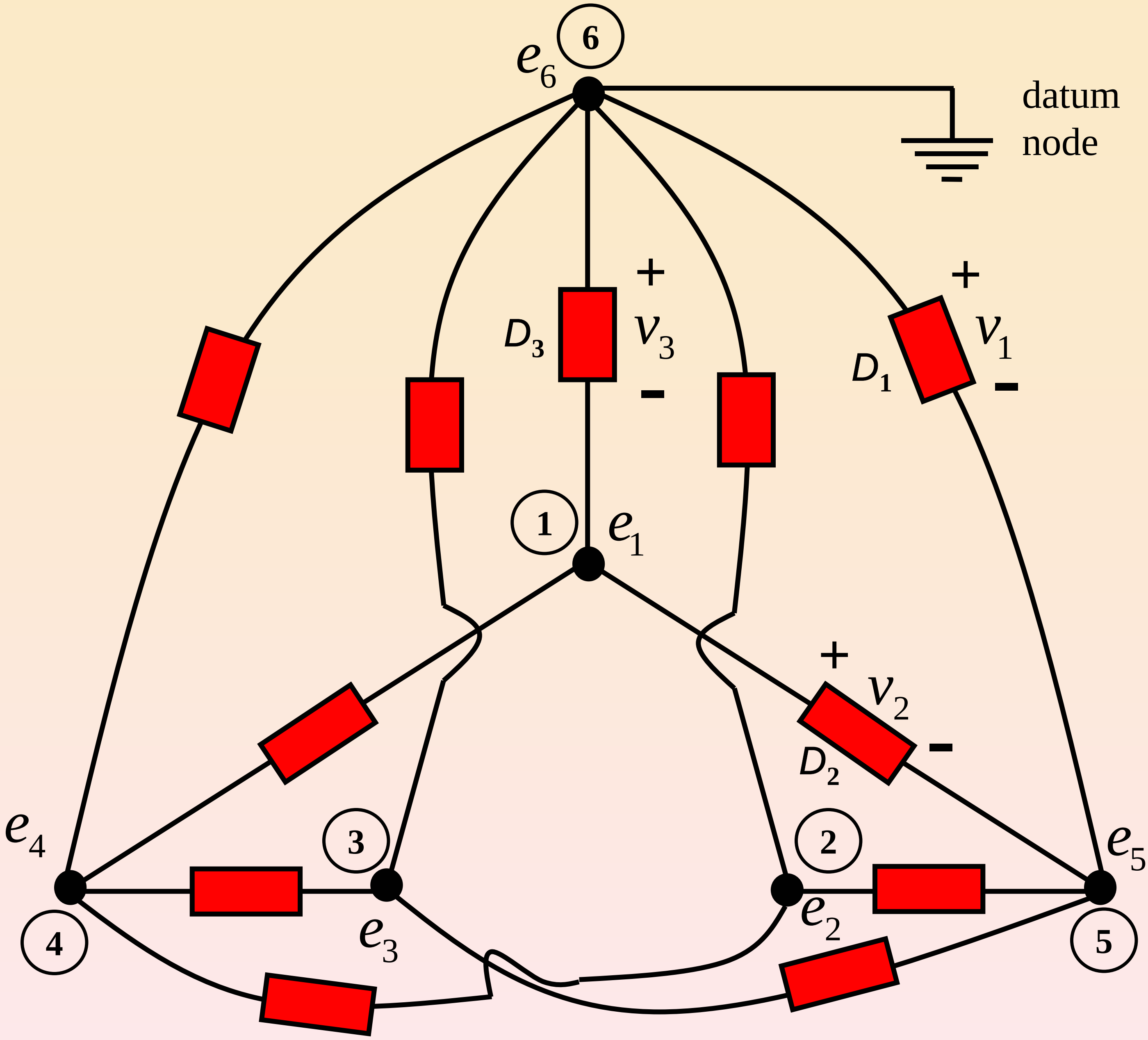
Algebraic sum of **all** voltages around any **loop** in a connected circuit is equal to **zero** at all times *t*.



KVL around loop

6 → 5 → 1 → 6 :

$$v_1 - v_2 - v_3 = 0$$

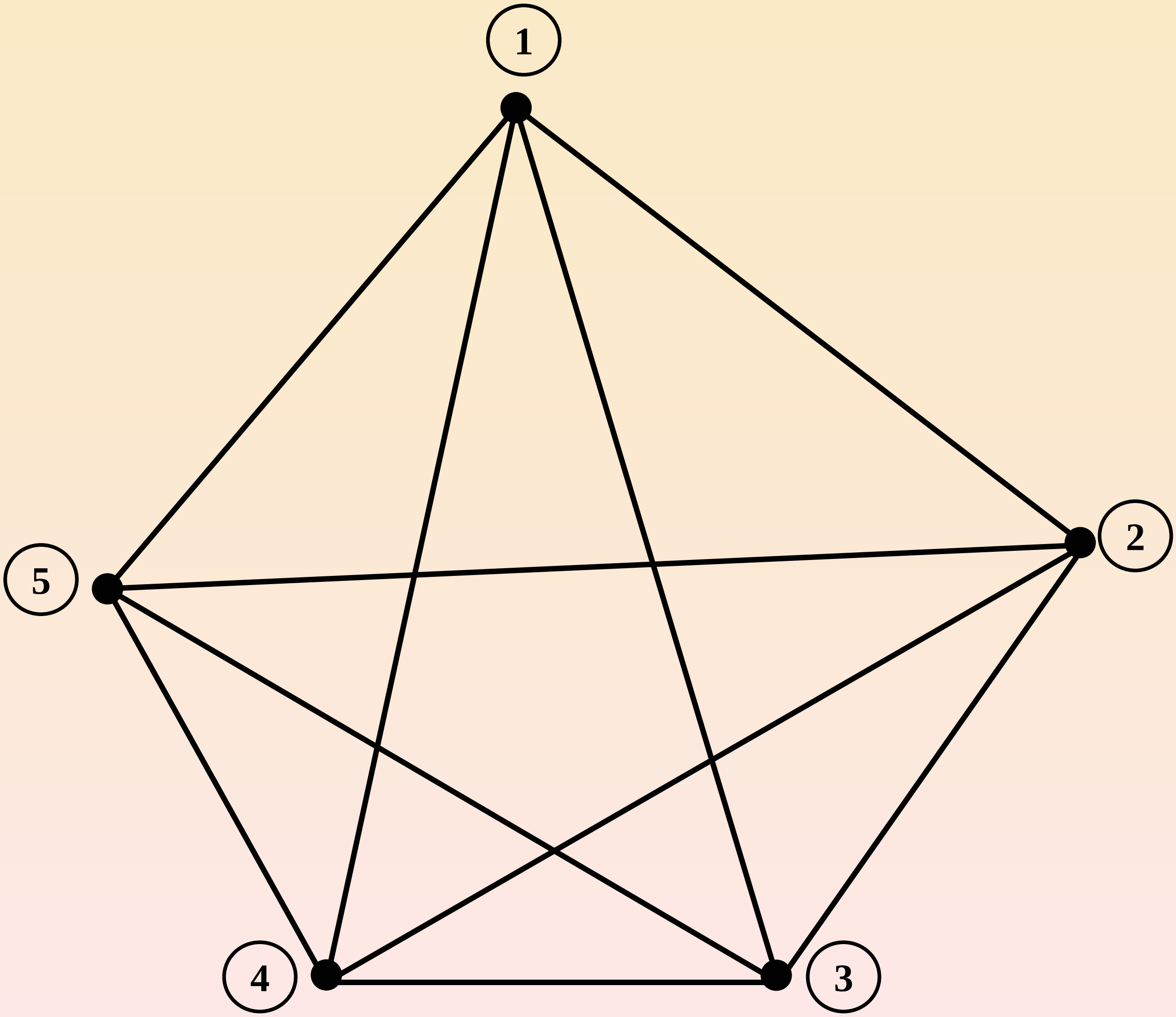


KVL around loop formed by the 3 devices

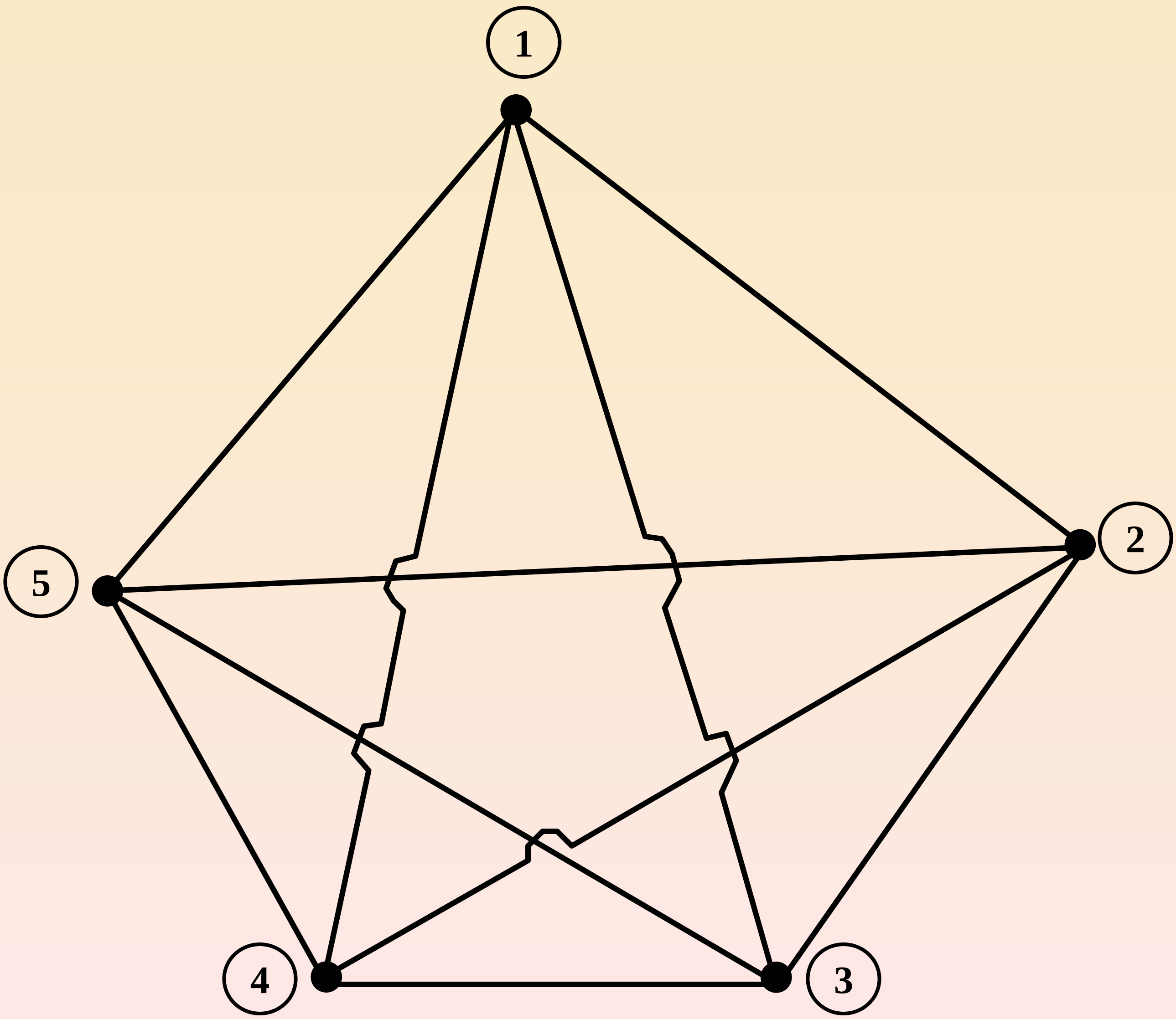
$$D_1 \rightarrow D_2 \rightarrow D_3 \rightarrow D_1 :$$

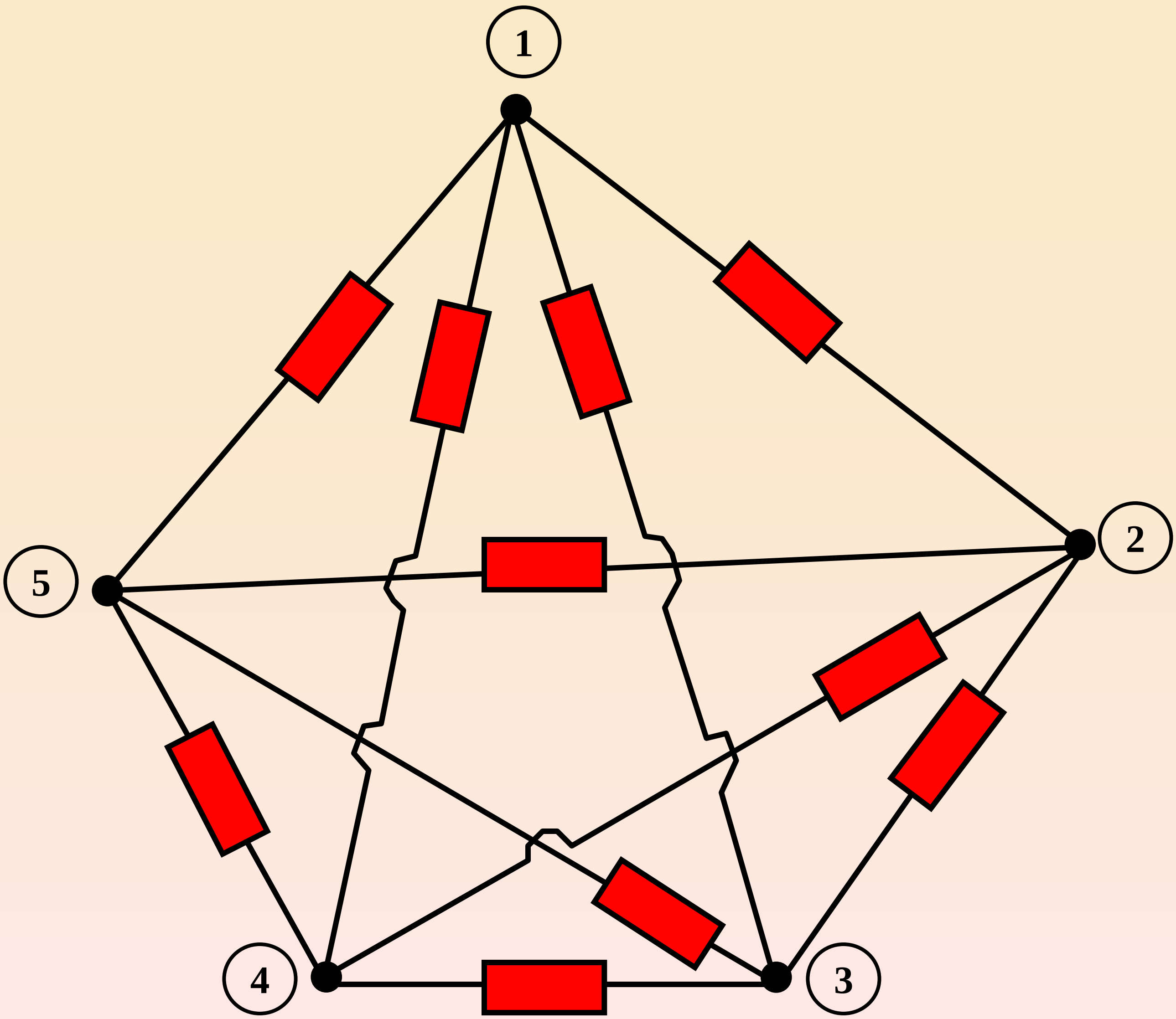
$$v_1 - v_2 - v_3$$

$$= (e_6 - e_5) - (e_1 - e_5) - (e_6 - e_1) = 0$$



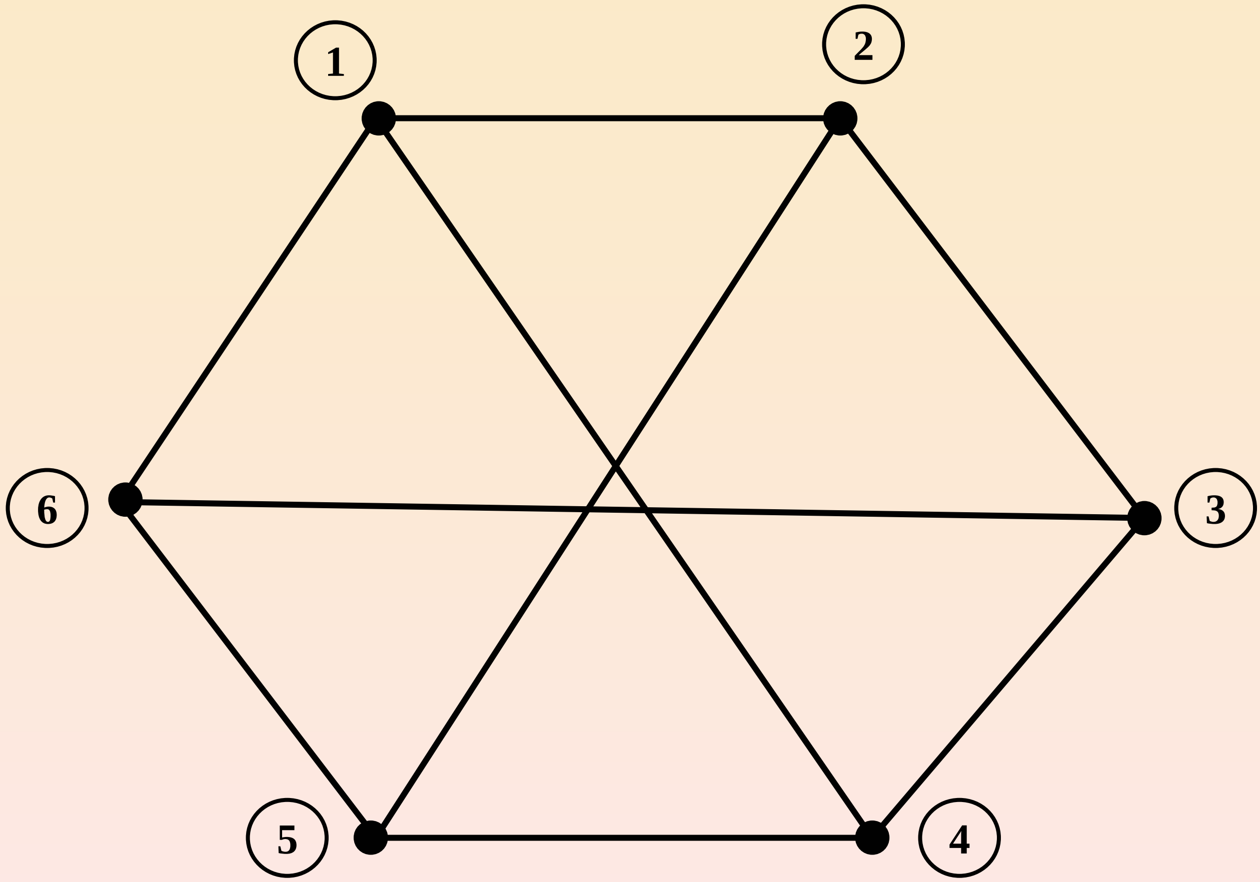
Basic Nonplanar Graph 1


1
2
3
4
5

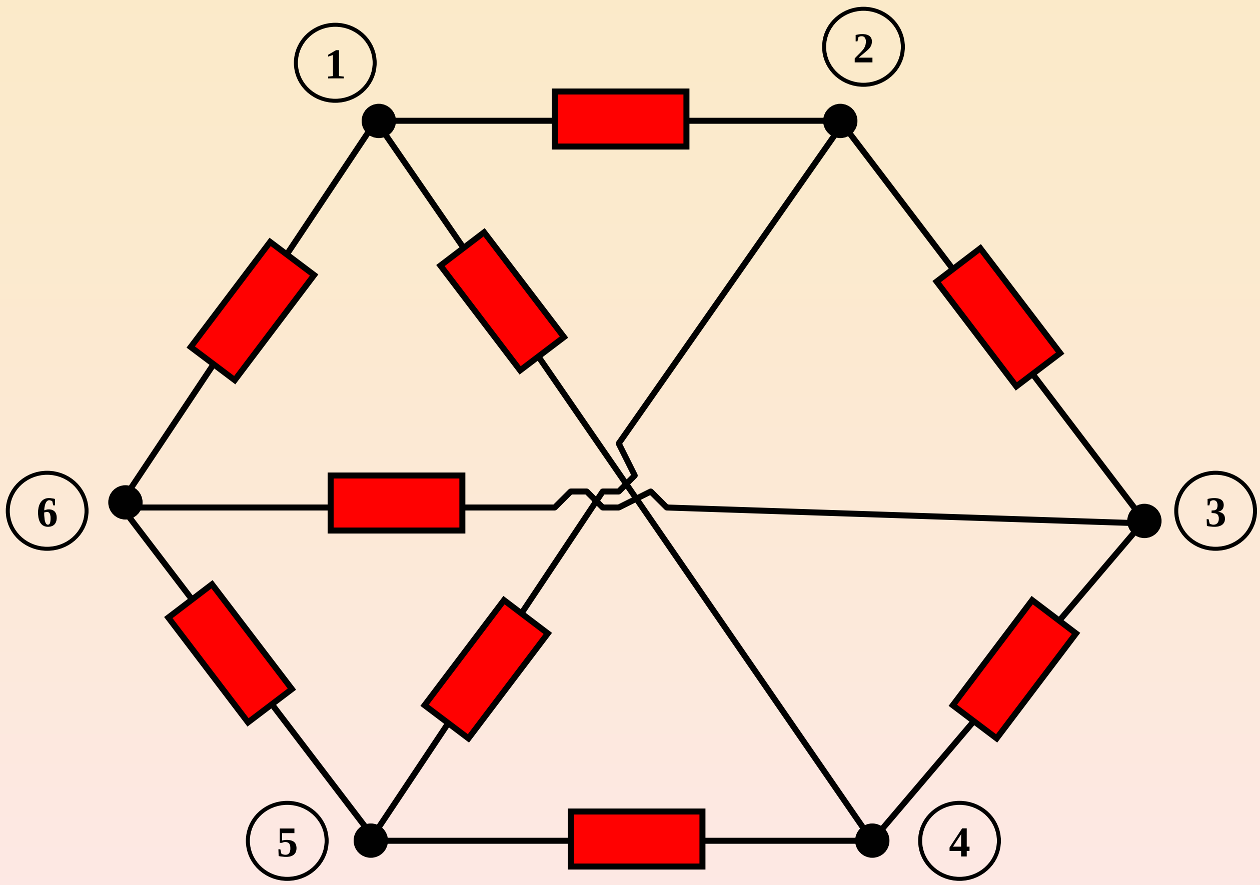


It is impossible to redraw this circuit without intersecting wires.

Hence, we can not define meshes in this circuit.



Basic Nonplanar Graph 2



It is impossible to redraw this circuit without intersecting wires.

Hence, we can not define meshes in this circuit.

How to test for Planar *G*

Kuratowski's Theorem

A **necessary** and **sufficient condition** for *G* to be a **planar graph** is that it does not contain either **Basic Nonplanar *G*raph 1** or **Basic Nonplanar *G*raph 2**, as a subgraph.

Remark

We can define **meshes** in a circuit iff its associated graph is planar

Definition:

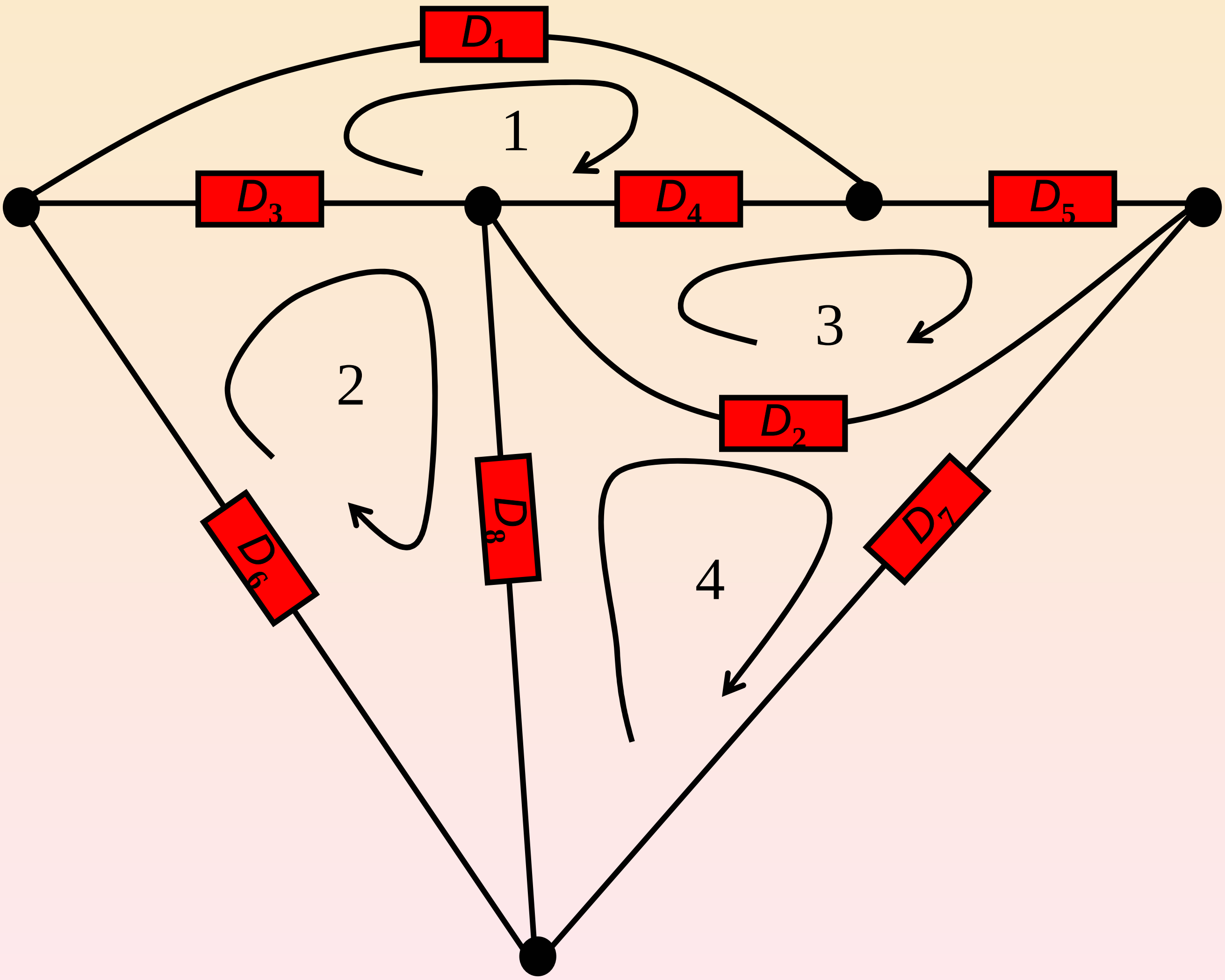
Planar Graph G

A graph G is said to be **planar** iff G can be **redrawn** on a plane with ***no intersecting branches except at the nodes***.

Mesh

Any loop formed by branches of a circuit is called a **mesh** iff the loop encloses **no other** branches, or wires in its interior.

A **Mesh** is like a **window**.



There are 4 **meshes** in this circuit.

Every mesh is a loop, but **NOT all loops are meshes**!