EE-100 Lab: Astable, Monostable, and Bistable op amp circuits - Theory

1. Objective

In this laboratory measurement you will learn about *oscillation mechanism* and *nonlinear wave shaping*. You will measure simple oscillatory and bi-stable flip-flop circuits.

2. Introduction: oscillators

Oscillation is a very natural phenomenon and you can see many different examples including physics, biology, chemistry, and electronics as well. Oscillators are used in many electronic devices (computers, radios, quartz watches, wireless devices, etc). Their common purposes are to generate a periodic signal. Every oscillator has at least one active device acting as an amplifier. All rely on the same basic principle: employing an amplifier whose output is fed back to the input in phase. Thus, the signal regenerates itself. This is known as a positive feedback in contrast to previous laboratory experiments where we used always negative feedback in op-amp circuits.

In this experiment we will focus on a special type of oscillators called *relaxation oscillator*. A relaxation oscillator is a circuit that repeatedly alternates between two states with a period that depends on the charging of a capacitor. The capacitor voltage may change exponentially when charged or discharged through a resistor from a constant voltage, or linearly through a constant current source. Next we will examine a simple circuit that can be easily transformed to an oscillator or a bi-stable flip-flop.

3. Negative resistance converter

Consider the following circuit shown in Figure 1:

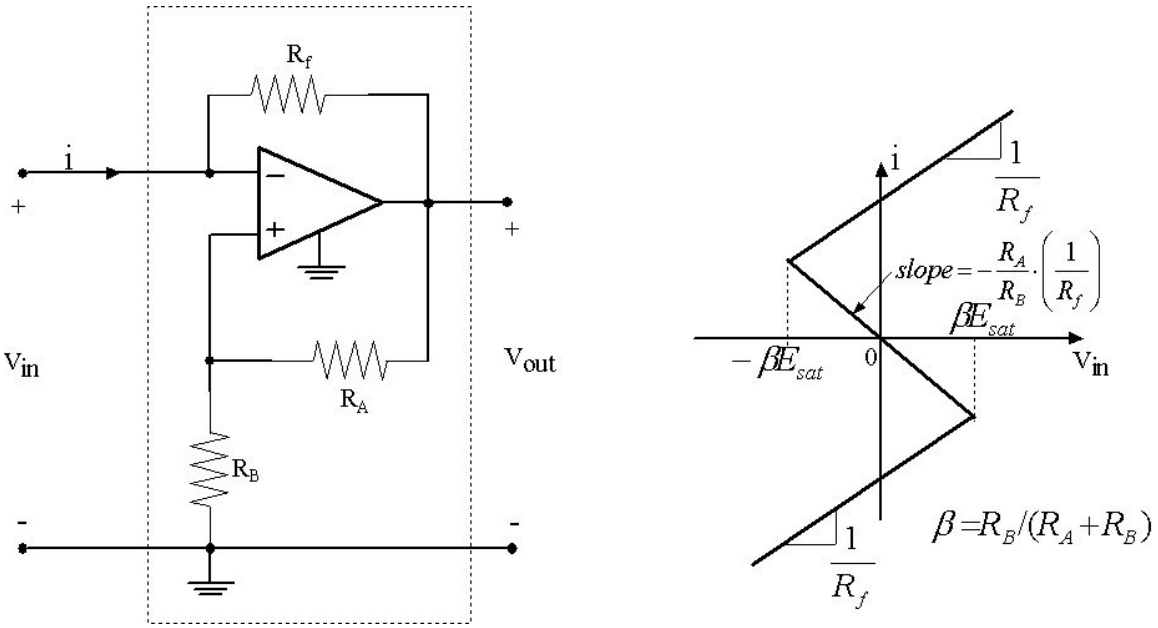

Figure 1 (a) A negative resistance converter and (b) its driving-point transfer characteristic.

This circuit realizes a *negative resistance converter* incorporating both a *negative* feedback path (via R_f) and a *positive* feedback path (via R_A). We will derive its driving

characteristic by inspecting both the linear and the saturation regions as well. First assuming that the circuit works in the linear region, we note that the R_A and R_B form a voltage divider so that

$$v_{in} = \frac{R_B}{R_A + R_B} \cdot v_{out} = \beta \cdot v_{out} \qquad \textbf{Eq 1}$$

We assumed ideal op-amp model so the voltage across R_B is equal to v_{in}. Applying KVL we obtain

$$v_{in} = R_f \cdot i + v_{out} \qquad \textbf{Eq 2}$$

Substituting Eq1 into Eq2 and solving for *i*, we obtain

$$i = -\left(\frac{R_A}{R_B}\right)\left(\frac{1}{R_f}\right) \cdot v_{in} \qquad \textbf{Eq 3}$$

Eq 3 is drawn as the middle segment in Figure 1-b). The boundary of this segment can be obtained by substituting Eq 1 into the validating inequality $|v_{out}| < E_{sat}$ so that

$$-\beta E_{sat} < v_{in} < \beta E_{sat} \qquad \textbf{Eq 4}$$

By inspection of the positive saturation region ($v_{out} = E_{sat}$), we find that

$$v_{in} = R_f \cdot i + E_{sat}, \text{so we get } i = \frac{1}{R_f} \cdot v_{in} - \frac{E_{sat}}{R_f} \qquad \textbf{Eq 5}$$

Eq 5 defines the lower segment in Figure 1-b). By inspection of the negative saturation region and following the same procedure as above, we obtain

$$i = \frac{1}{R_f} \cdot v_{in} + \frac{E_{sat}}{R_f} \qquad \textbf{Eq 6}$$

This equation defines the upper segment in Figure 1-b).

This circuit is called a *negative-resistance converter* because it converts positive resistance R_A, R_B, and R_f into a negative resistance equal to $-R_f \cdot \frac{R_B}{R_A}\Omega$ in the linear region. Next we show how this circuit can be easily transformed into an oscillator.

4. Relaxation oscillator

Let us connect a capacitor across the input terminals of the negative resistance converter. Such a circuit is shown in Figure 2. Its driving point characteristic was derived earlier in Figure 1. Let us consider the four different initial points Q_1, Q_2, Q_3, and Q_4 (corresponding to four different initial capacitor voltages at $t = 0$) on this characteristic. Since $\dot{v}_{in}(t) = \dot{v}_c(t) = -i(t)/C$ and $C > 0$, we have

$\dot{v}_{in}(t) > 0$ for all t such that $i(t) < 0$,

and $\dot{v}_{in}(t) < 0$ for all t such that $i(t) > 0$.

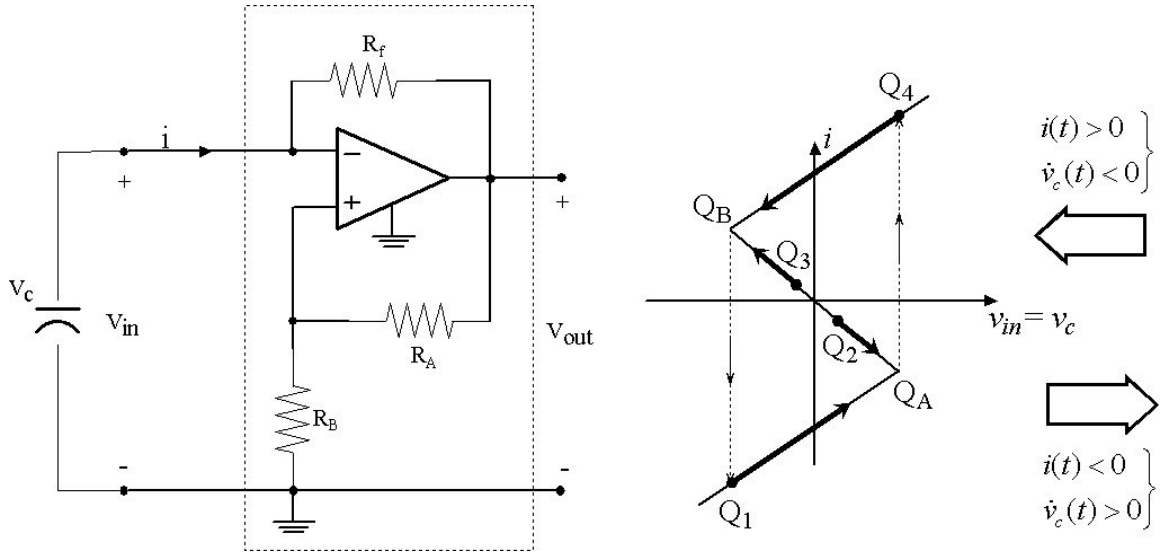

Figure 2 (a) An astable RC op-amp circuit and (b) its driving-point characteristic

Hence the *dynamic route* from any initial point must move *toward the left in the upper half plane*, and *toward the right in the lower half plane*, as indicated by the arrow heads in Figure 2 (b). Observe that there is no stable equilibrium point in the circuit because the zero i current belongs to an unstable equilibrium (opposite arrowheads diverging from zero). This equilibrium point cannot be observed in practice, because any small amount of noise will drive out the circuit from this point. Also, the breakpoints Q_A, and Q_B cannot be equilibrium points because $i \neq 0$. Since, arrowheads towards Q_A, and Q_B are oppositely directed it is impossible to continue drawing the dynamic route beyond Q_A, or Q_B. In other words, an *impasse* is reached whenever the solution reaches Q_A, or Q_B.[1] The dotted arrows show that a sudden *instantaneous transition* will occur (also called *jump*). For an *RC* circuit this transition should be always a vertical jump (assuming in the *v-i* plane that i is the vertical axis) because the voltage across a capacitance cannot be changed suddenly such that $v_c(T^+) = v_c(T^-)$. Applying jumps at the two *impasse* points Q_A, and Q_B we obtain a closed dynamic route. This means that the solution waveforms become *periodic* after a short transient time (starting from any initial capacitance voltage) and the op-amp circuit functions as an *oscillator*. Note that the oscillation is not sinusoidal. Such oscillators are usually called *relaxation oscillators*.

To figure out what kind of waveforms will be generated note that the closed dynamic route operates always in the saturation regions (except for the short transient time at the very beginning). These are the segments Q_1-Q_A, and Q_4-Q_B. It means that the output voltage (v_{out}) will alternate between the two saturation levels, $+E_{sat}$ and $-E_{sat}$. The output will be a square wave with a duty cycle of 50 % if the saturation levels are symmetrical.

[1] Any circuit which exhibits an impasse point is the result of poor modeling. This impasse point can be resolved, for this circuit, by inserting a very small linear inductor (representing the inductance of the connecting wires) in series with the capacitor.

Since the output voltage will be either $+E_{sat}$ or $-E_{sat}$, then the non-inverting input of the op-amp will be biased at $\beta \cdot E_{sat}$ or $-\beta \cdot E_{sat}$. This will drive the circuit to behave as a comparator. Until the voltage of the capacitance is lower than $\beta \cdot E_{sat}$ the output will remain at $+E_{sat}$, and similarly until the voltage of the capacitance is larger than $-\beta \cdot E_{sat}$ the output will be always $-E_{sat}$. The capacitor voltage will change exponentially because it is charged or discharged through the resistor R_f from a constant voltage $+E_{sat}$ or $-E_{sat}$, respectively. The Figure 3 shows the expected waveforms.

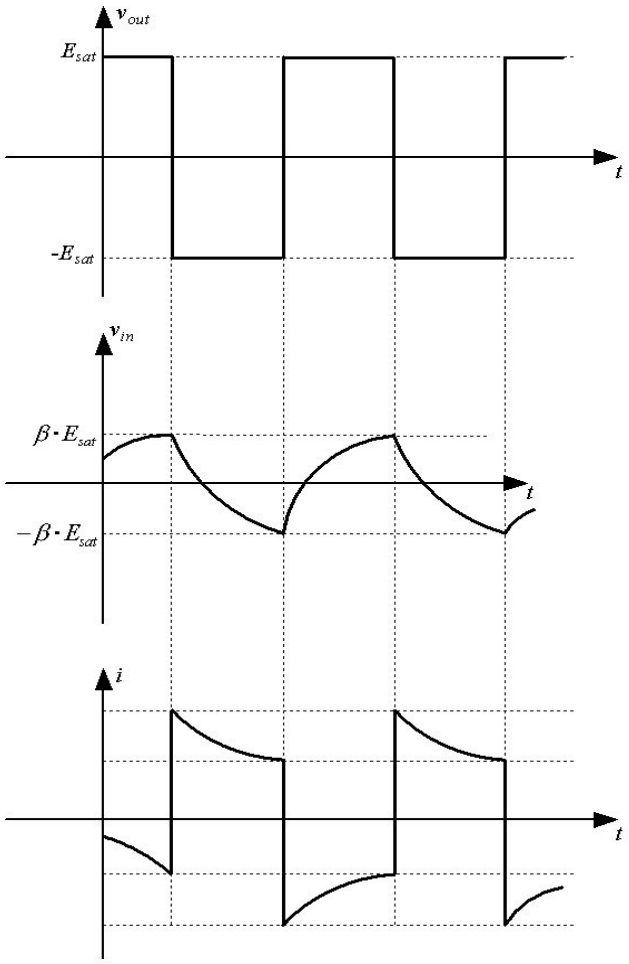

Figure 3 Waveforms of RC op-amp circuit, (a) output voltage, (b) input voltage, (c) input current

Observe that this RC op-amp circuit is *autonomous* in the sense that it produces periodic oscillatory signal without any external driving periodic signal (compare to the previous lab measurement: designing a poor man's square wave generator).

5. Bistable circuit (flip-flop)

Now suppose we replace the capacitor in Figure 2 by an inductor-voltage source combination as shown in Figure 4-a). Let us consider first the case when $v_s(t) = 0$ so the inductor is directly connected across the inverting terminal of the op-amp and the ground. Since $di/dt = -v_{in}(t)/L$ and $L > 0$, it follows that

$di / dt > 0$ whenever $v_{in} < 0$
and $di / dt < 0$ whenever $v_{in} > 0$.

Hence the current *i decreases* in the right half *v-i* plane and *increases* in the left half *v-i* plane, as shown by dynamical routes in Figure 4-b).

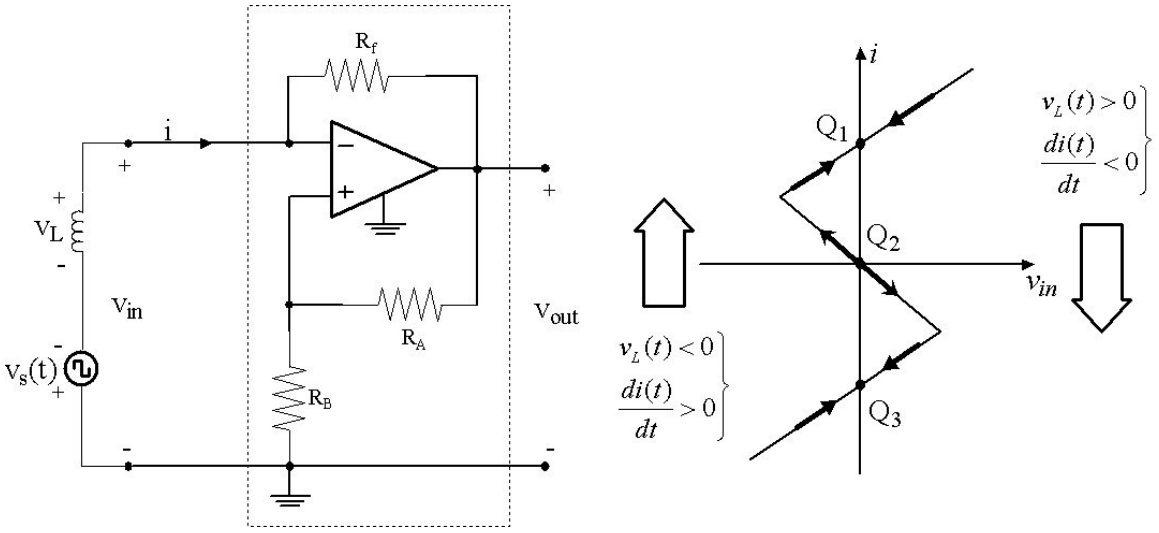

Figure 4 (a) A bi-stable op-amp circuit and (b) its driving point characteristic

Since the equilibrium state of a first-order RL circuit is determined by replacing the inductor by a short circuit, i.e. $v_{in} = v_L = 0$, it follows that this circuit has three equilibrium points; namely, Q_1, Q_2, and Q_3. These equilibrium points are now the operating points of the negative resistance converter. Since the dynamic route always diverges from Q_2, therefore this equilibrium point is *unstable*. This can never be observed in practice – the slightest noise voltage will cause the dynamic route to diverge from Q_2. The other two equilibrium points are stable (converging arrow heads). Whether Q_1 or Q_3 is actually observed depends on the initial condition. Such a circuit is said to be *bistable*.

Switching a bistable circuit requires a proper triggering signal. In our case the $v_s(t)$ will accomplish this task. Applying a square pulse the inductor will see a translated driving-point characteristic that will be shifted left or right depending on the polarity of the square pulse.

Suppose initially the circuit is operating at Q_1. Let us at $t = t_1$ apply a *square pulse* of width $T = t_2 - t_1$ as shown in Figure 5-a). During the time interval $t_1 < t < t_2$, $v_s(t)$ can be replaced by an *E-V* battery, so that the inductor sees a translated driving-point characteristic as shown in Figure 5-b) in broken line segments. Since the inductor current cannot change instantaneously [$i_L(t_{1-}) = i_L(t_{1+})$], the dynamic route must jump horizontally from Q_1 to P_1. From P_1 the current i must subsequently decrease so long as $v > 0$. Here, we assume that at time $t = t_{2-}$, the dynamic route arrives at some point P_3 in the lower half plane. At time $t = t_{2+}$, the dynamic route must jump horizontally back to its original position. For successful triggering the amplitude of the triggering signal should

satisfy the condition $E > \beta E_{sat}$ and the minimum pulse width should be longer than time needed for the dynamic route to reach the lower half plane (P_2). To trigger from Q_3 back to Q_1, simply apply a similar triggering pulse of *opposite* polarity.

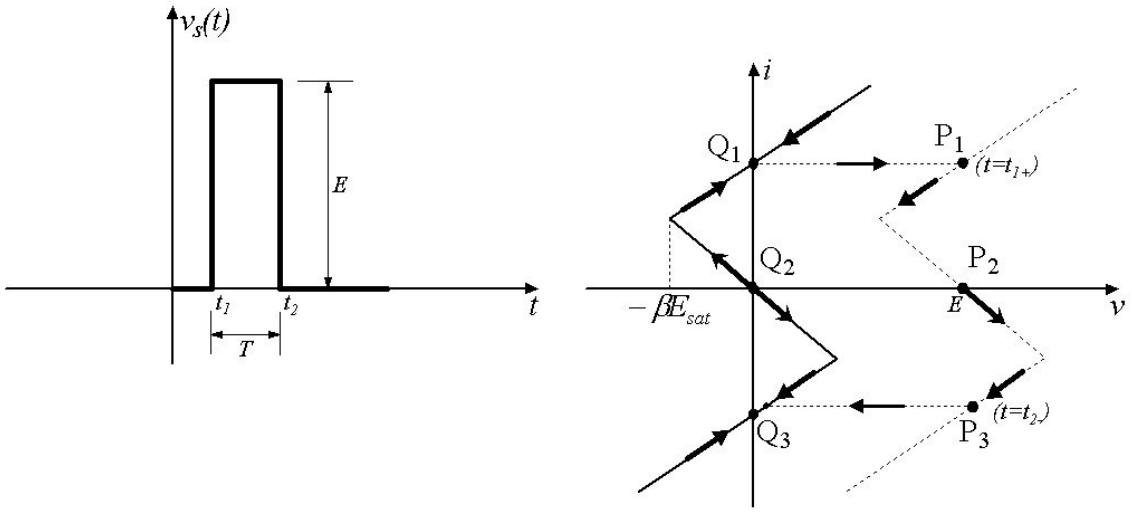

Figure 5 Dynamic route of the bistable op-amp circuit corresponding to a typical square pulse triggering signal

Triggering criteria – The following two conditions must be satisfied by the triggering signal in order to trigger from Q_1 to Q_3, or vice versa.

a) **Minimum pulse width condition** – The pulse width cannot be shorter than the time required for the dynamics to reach the horizontal *v* axis.

b) **Minimum pulse height condition** – the amplitude of the pulse should be larger then the boundary of the linear region (i.e. βE_{sat}).

EE-100 Lab: Astable, Monostable, and Bistable op amp circuits – Experiment Guide

Exp 1 – Negative resistance converter:
Build a negative resistance converter (Figure 1). Let R_A, R_B, and R_f be 10k, 10k, and 4.3k, respectively. Connect a 1μF capacitor across the inverting terminal of the op-amp and the ground.
If you are using a dual or quad op-amp IC, be sure to ground the unused op-amps (refer to the op-amp lab measurement guide). You must refer to the datasheet of the particular IC you will be using to find out which pins on the IC package connect to which nodes. (Hint: the AD823 op-amp is more robust for this measurement than other type of op amps.) Use V_{DD}=12V and V_{SS}= -12V (on the datasheet these are called $+V_S$ and $-V_S$). Refer to the basic lab experiment on how the power supply should be connected!

Exp 1 – Oscillation (astable circuit measurement):
1-a) Output measurement: Switch on the circuit. Observe the output signal. What does the waveform look like? Characterize it (amplitude, frequency, duty cycle). Is it possible to change the duty cycle? How?

1-b) Input voltage measurement: Observe both the input voltage and the output voltage. What are the comparator levels?

1-c) Input current measurement: Observe both the input voltage and the input current. What are the maximum current levels? *Hint: to measure the input current choose an appropriate resistor voltage related to this current. To observe both input current and input voltage, note that the scope cable is grounded and the channels cannot be floating independently. The scope ground should not be the ground of this circuit.*

1-d) Driving-point characteristic: Measure the input current versus to the input voltage. Set the scope to display the driving-point characteristic (X/Y mode). What does the driving-point characteristic look like? Explain. Which part of the driving-point characteristic is visible? Why? *Hint: Figure 2-b can help.*

1-e) Parameter dependency measurement: Change R_B to 4.3k. How the waveform has changed (frequency, comparator levels, etc)? Set back R_B to 10k and change R_f to 10k. Repeat the measurement. Now change the capacitance to 4.7 uF or 10 uF. Repeat the measurement. Explain the reasons of these changes!

Exp 2 – bi-stable (flip-flop):
Connect a 4700 μH inductor directly across the inverting terminal of the op-amp and the ground (Figure 4). *Do not connect any additional voltage source yet.*

2-a) Operating point measurement: Switch on the power supply and measure the output voltage. Repeat several times this measurement by switching on and off the power supply. Do you get different output voltages or not? What might be the reason for this

behavior? Which operating point (Q_1, Q_2, Q_3) is actually observed? Relate operating points to output voltages.

2-b) Manual triggering: Now, connect a DC source - $v_s(t)$ – in series with the inductor. Start from zero voltage and increase its voltage slowly to positive or negative direction. Measure the output voltage continuously. Record the voltage level when the circuit switches from Q_1 to Q_3, and vice versa. What polarity of triggering signal is needed to switch from positive saturation to negative, and vice versa?

2-c) Periodic triggering: Replace the DC source with an AC source. Set the input signal to 1 kHz, 500mV V_{PP}, 0.0 VDC offset sine wave from the function generator. Increase the amplitude and measure the minimum pulse height to trigger the bi-stable circuit. Is this same as the previous result? Now, decrease the triggering pulse width by increasing the frequency. What is the minimal pulse width to trigger this bi-stable circuit?

2-d) Parameter dependency: Change R_f to 1k. How the triggering criteria have changed? Change R_B to 1k and repeat the measurement. Try to give a reasonable explanation.