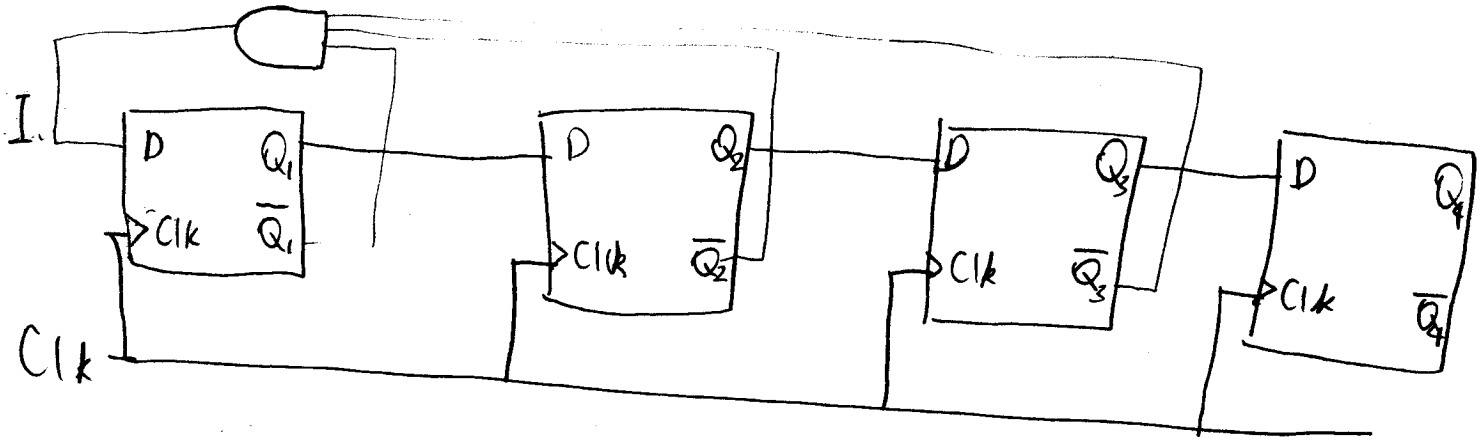
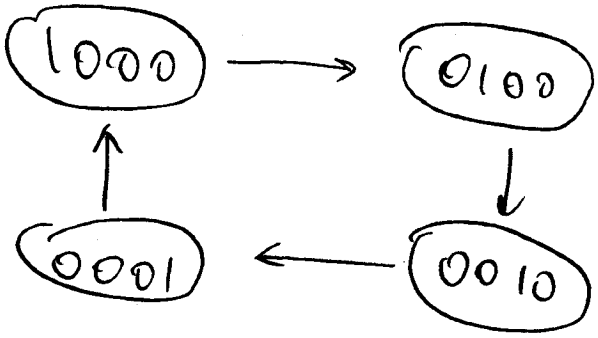
EE 100 HW 12 Solns



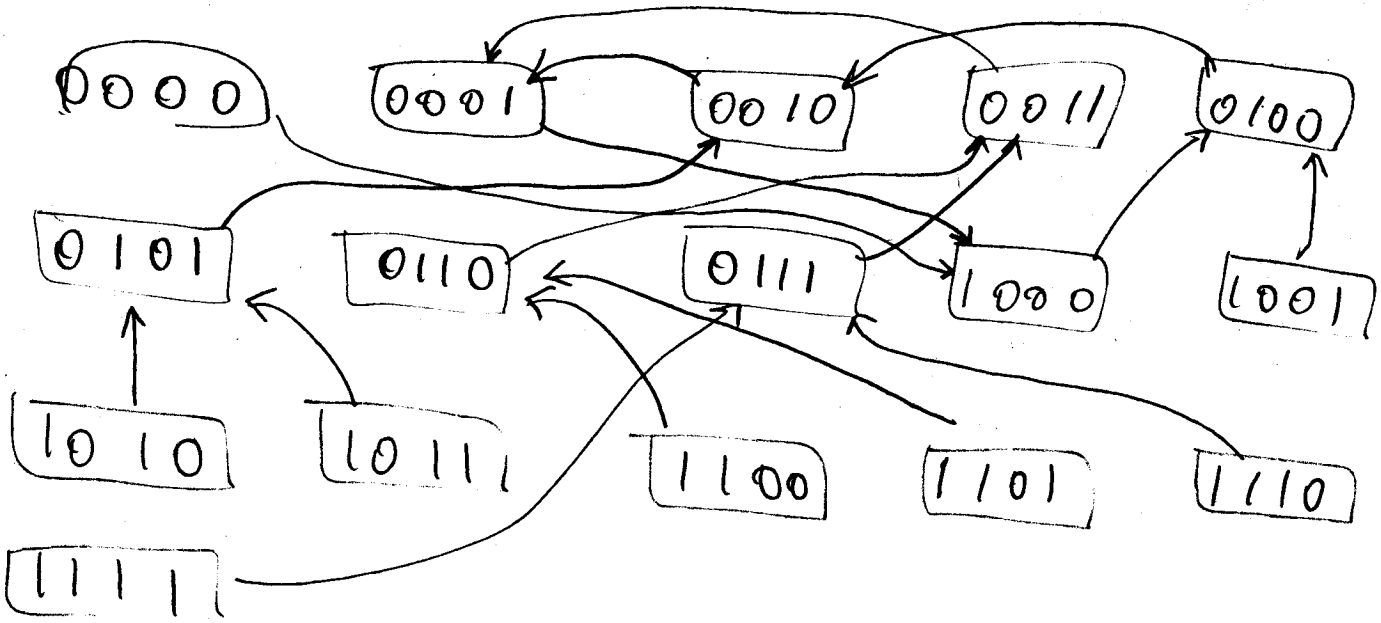
2a) Initially $Q_1 = 1$, $Q_2 = Q_3 = Q_4 = 0$

N	Q_1	Q_2	Q_3	Q_4	I
0	1	0	0	0	0
1	0	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	1
4	1	0	0	0	0

b)



3)

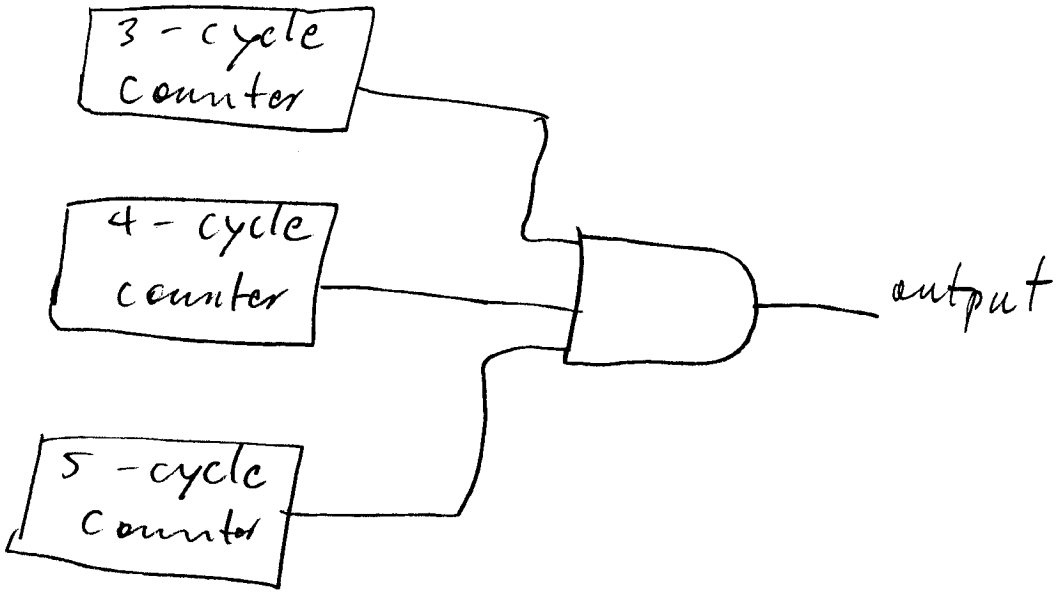


Limit Cycle : 1000 → 0100 → 0010 → 0001 → 1000

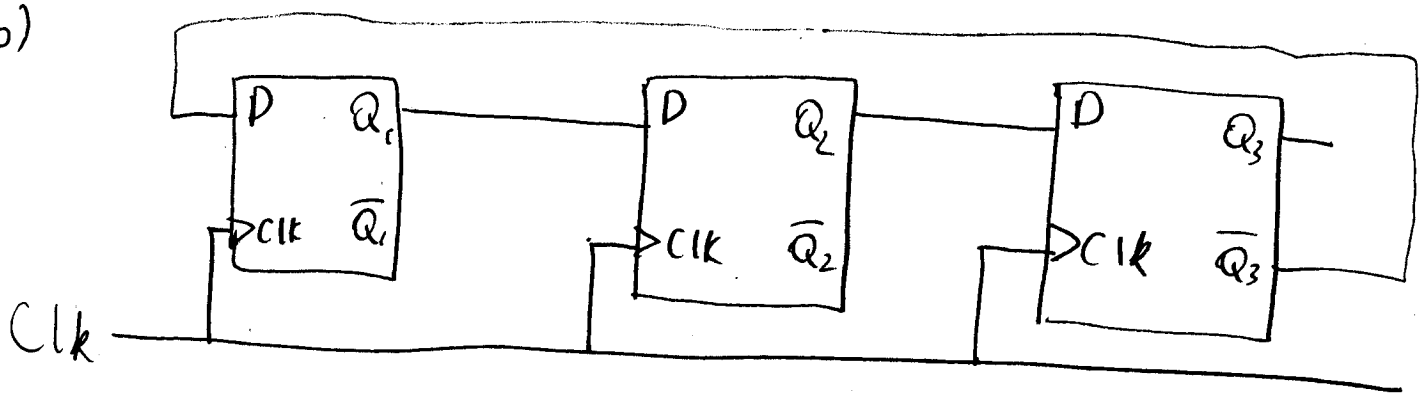
4) Looking at the state table in #2 and starting w/ when I is 1 (state 0001) we see that I is I after every fourth clock pulse after.

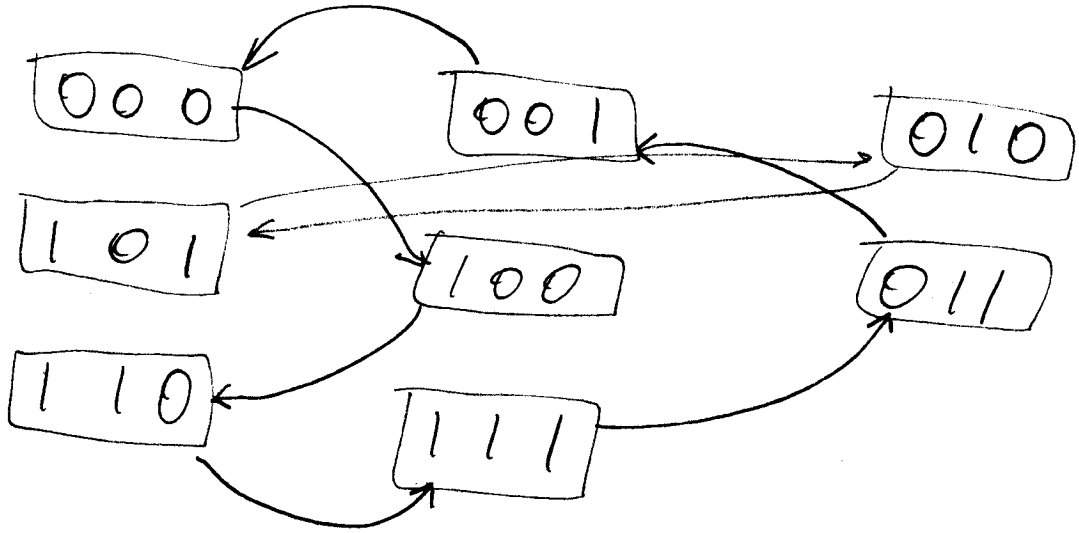
To give an output of 1 after every fifth clock pulse, we can add another flip-flop to the chain.

5) From previous questions, we see that the way to build an n-cycle counter is to have n flip-flops and an n-1 input AND gate. If we want to use less (as stated in this question) we can use an AND gate to combine the output of 2 or more counters, such the final output is only high when all the outputs of the counters are high (in other words, a common multiple) In this case we want the LCM of our counters to be 60. In order to use less than 12 flip-flops, we can have a design like this;



6)



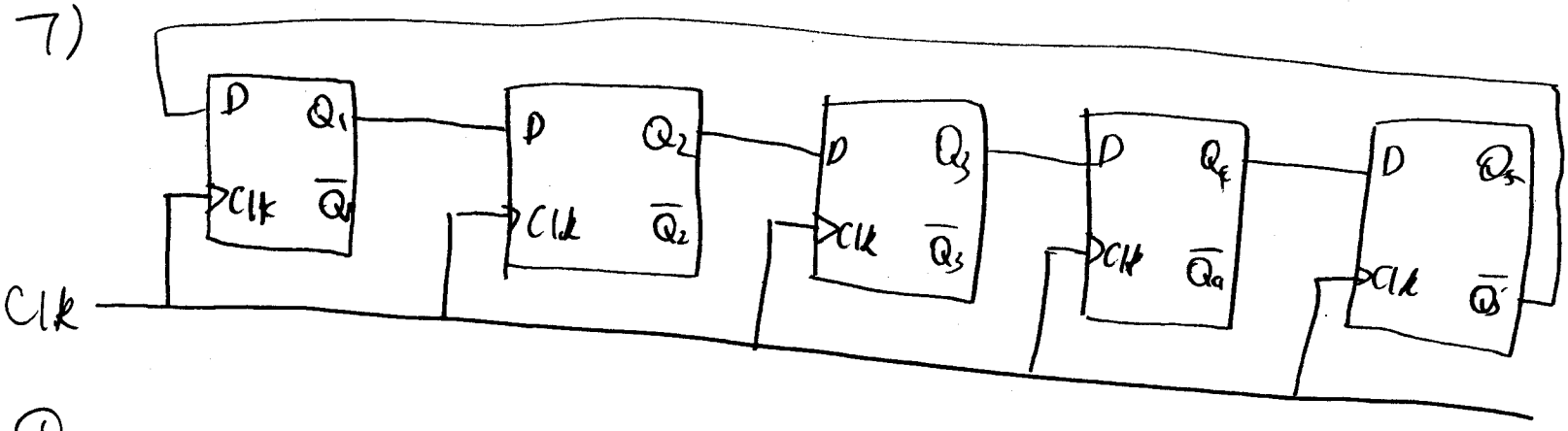


Cycle 1: 000 → 100 → 110 → 111 → 011 → 001 → 000

Cycle 2: 101 → 010 → 101

We can use an AND gate to combine Q_1, Q_2, Q_3 ⇒ it will only give a 1 when all of them are 1, which is once every 6 cycles according to Unit cycle 1.

7)



① 00000 → 10000 → 11000 → 11100 → 11110

↓

00001 ← 00011 ← 00111 ← 01111 ← 11111

② 01010 → 10101 ← contain 2 state

③ 00100 → 10010

↑ ↓

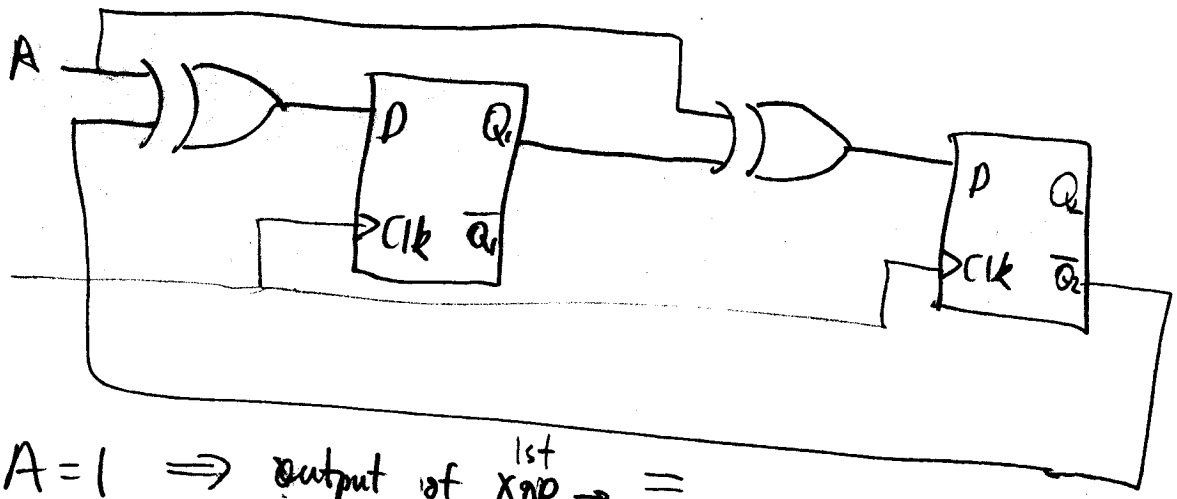
11001

④ 10001 → 01000 → 10100 → 11010 → 11101

↑ ↓

00010 ← 00101 ← 01011 ← 10111 ← 01110

8)



XOR

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

a) $A=1 \Rightarrow$ output of 1st XOR $\rightarrow \overline{\overline{Q_2}} = Q_2$

2nd XOR $\rightarrow \overline{Q_1}$

N	Q_1	Q_2
0	0	0
1	0	1
2	1	1
3	1	0
4	0	0

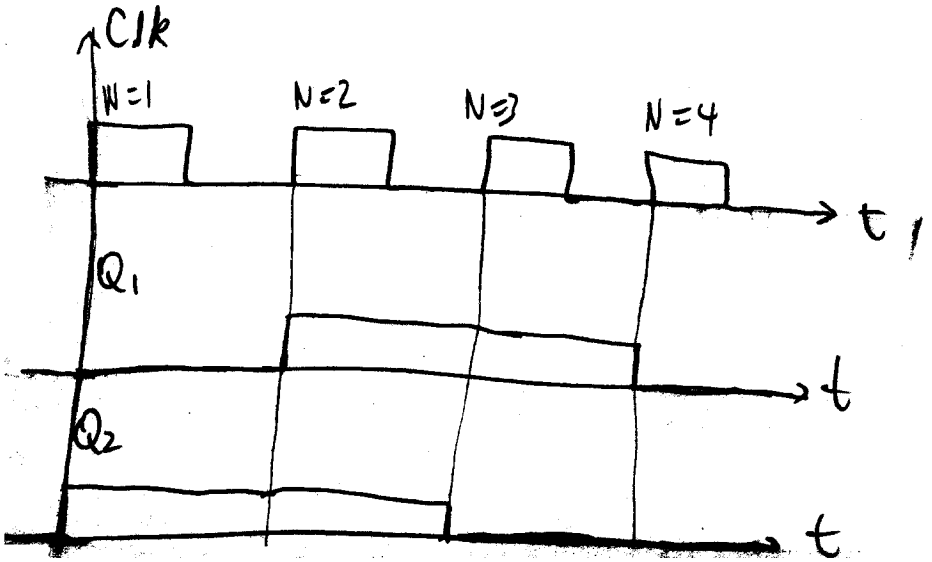
b) $A=0 \Rightarrow$ output of 1st XOR $\rightarrow \overline{Q_2}$

2nd XOR $\rightarrow Q_1$

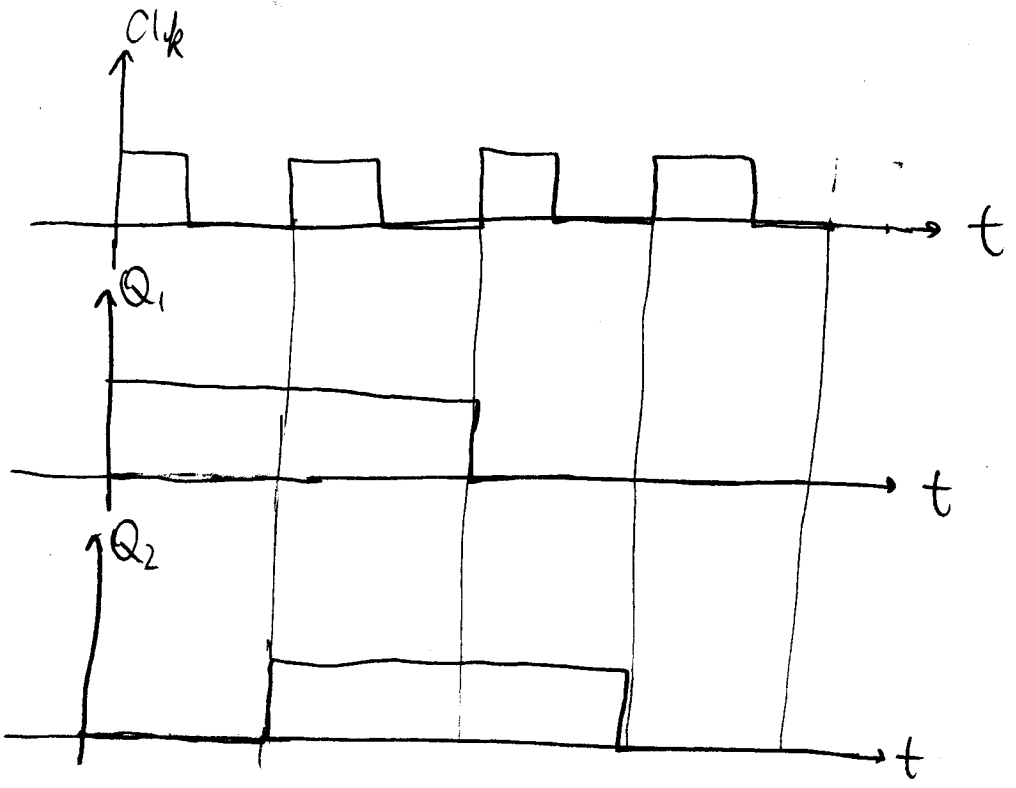
N	Q_1	Q_2
0	0	0
1	1	0
2	1	1
3	0	1
4	0	0

c)

A=1



8) c)



d) Q_1 and Q_2 are swapped in the 2 cases

9) We want a D to A Converter (DAC) that outputs 10V when all the bits are high

Since the input voltages to the op amps are the same, and each binary number represents a multiple of 2, we have for Vout

$V_{out} = (2^0 + \cdots + 2^7) \cdot$ Supply voltage $\cdot$ Ratio of resistor of summing amp

$10V = (2^8 - 1) \cdot \frac{x}{y}$ ← supply, $\frac{x}{y}$ ← ratio of resistors

$10V = 255 \frac{x}{y}$

$\frac{x}{y} = \frac{2}{51} \Rightarrow$ see design on right hand side