The Word version only operates on the rightmost 12 bits of a 64-bit registers.

2) Operation assumes unsigned integers (instead of 2's complement).

3) The least significant bit of the branch address in iar is set to 0.

4) (signed) Load instructions extend the sign bit of data to fill the 64-bit register.

5) Replicates the sign bit to fill in the leftmost bits of the result during right shift.

6) Multiply with operand signed and one unsigned.


8) Classify a 10-bit mask to show which properties are true (e.g., -inf, 0, +inf, denorm, ...).

9) Atomic memory operation; nothing else can interfere itself between the read and the write of the memory location.

The immediate field is sign-extended in RISC-V.