Hamming Codes
Recall the basic structure of a Hamming code. Given bits 1...,m, the bit at position 2^n (starting at n=0, the first bit) is parity for all the bits with a 1 in position n. For example, the first bit is chosen such that the sum of all odd-numbered bits is 1.

Exercise:
1. Suppose you had the bits 0011 and we want to add some bits to allow single error correction.
a) How many bits do we have to add? 3

b) Which bits are parity bits?
Parity bits are at positions labeled with x: XX0X011

c) Which bits does each parity bit cover?
bit 1 1,3,5,7
bit 2 2,3 6,7
bit 4 4,5,6,7

d) Write Hamming code for this bit string.
1000011

e) What do we need to do to make this into a SEC-DED code?
Add another parity bit over the whole sequence.

2. Find the original bits given the following SEC Hamming Code.
a) 0110111
Group 1 error
Group 2 ok
Group 4 error
The fifth bit should be a 0. 1011
b) 1001000
Group 1 error
Group 2 ok
Group 4 error
Fifth bit should be a 1. 0100

3. If we didn't need SEC but wanted SED, how bits would we need to add for 4 bits?
1

Set Associative Caches
How big should the T, I, and O fields of a memory address be on a system with…
a. 32-bit addressed memory, 64 KB fully associative cache, 4-byte blocks
30/0/2
b. 32-bit addressed memory, 64 KB fully associative cache, 16-byte blocks
28/0/4
c. 8-bit addressed memory, 32 B 2-way set associative cache, 4-byte blocks
4/2/2
d. 8-bit addressed memory, 32 B 4-way set associative cache, 4-byte blocks
5/1/2

(From Summer 98 final)

1. A 32kB cache has a linesize of 16 bytes and is 4-way set-associative. How many bits of an address will be in the Tag, Index, and Offset? Assume 32 bit addresses.
19 Tag bits, 9 Index, 4 Offset

2. In a 2-way set-associative cache, three addresses, A, B, and C, all have the same index but distinct tags. What is a minimum sequence of accesses which, if repeated, will maximize the miss rate in the cache if it uses the LRU replacement policy?
A,B,C

3. If the above sequence is repeated for a long period of time, what will the miss rate be if the cache uses an LRU replacement policy?
1 (all misses)

4. If the hit time is 1 cycle, and the miss penalty is 3 cycles, what will be the average memory access time (in clock cycles) for the LRU replacement policy using the above sequence?
4 cycles

5. What would be a better replacement policy?
MRU, random

6. What will the miss rate be for LRU replacement when the sequence is A B C C B A A B C C B A . . . ?
1/3