inst.eecs.berkeley.edu/~cs61c
CS61C : Machine Structures

Lecture 41:
Introduction to Reconfigurable Computing

Michael Le, Sp07 Head TA

April 30, 2007

Slides Courtesy of Hayden So, Sp06 CS61c Head TA

Following the tech news tradition…

NeuroSky of San Jose, CA aims to add more realistic elements to video games by using brain wave-reading technology to help game developers make gaming more realistic.

http://news.yahoo.com/s/ap/20070430/ap_on_hi_te/mind_reading_toys

Outline

- Computing… What does it mean?
- Processor vs ASIC
- FPGA-based Reconfigurable Computing
- Real stuff

Back to basics…

- What does the word "***computer***" mean to you?
  - Your $700 box sitting under your desk at home?
  - The $2000 laptop you are using to check email right now?
  - The 5-stage pipeline processor?

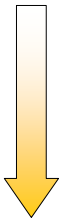
Informal Definition

- A computer is a machine that ***computes***
  - add, subtract, logical operations, decisions
- What have we learned about computing in this semester?

Calculating Class Grades*

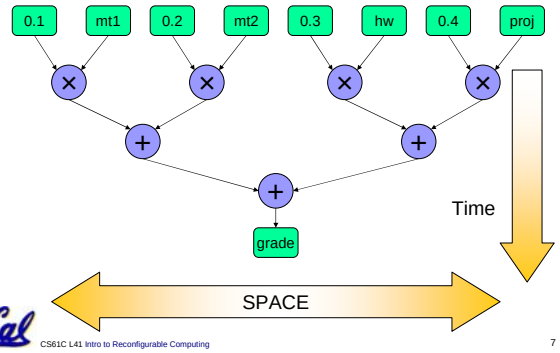
```
grade = 0.1 × mt1 + 0.2 × mt2
       +0.3 × hw + 0.4 × proj;
```

```
grade = 0;
tmp = 0.1 × mt1;
grade = grade + tmp;
tmp = 0.2 × mt2;
grade = grade + tmp;
tmp = 0.3 × hw;
grade = grade + tmp;
tmp = 0.4 × proj;
grade = grade + tmp;
```

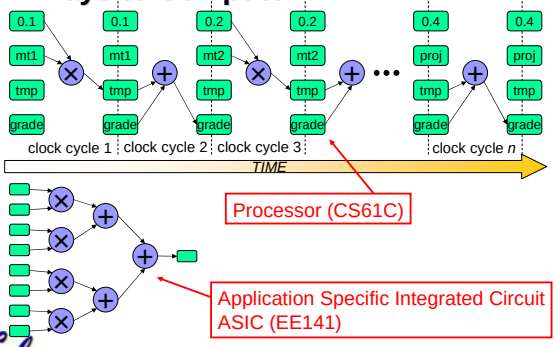


*This is not how we are going to calculate your grades

Computing Final Grade (2)



2 Ways to Compute



Processor vs ASIC

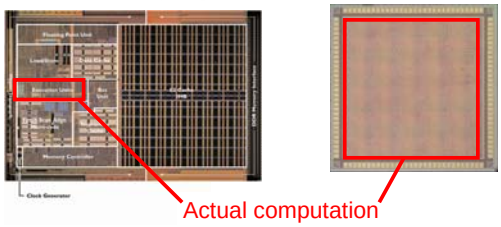
- Take longer to compute
  - slow
- Flexible
- Need instructions to determine what to do on each cycle
- Space is bounded

Temporal Computing

- Take shorter time to compute
  - fast
- Not Flexible
- No instruction
  - Same calculation every cycle
- Space unbounded
  - Branches?

Spatial Computing

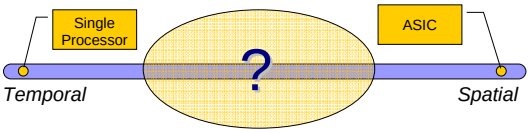
Visualizing Spatial Computing



- AMD Opteron 64-bit processor
  - 1MB L2 Cache
- 193 mm sq
  - 0.18 micron CMOS
- 89W @ 1.8GHz
- ~3 Op / cycle (int op)

- Full Custom ASIC
  - 4x4 Single Value Decomposition
- 3.5 mm sq
  - 90nm CMOS
- 34mW @ 100 MHz clock
- 70 GOPS = 700 Op / cycle

Between Temporal & Spatial Computing



- Slow
- Flexible

Reconfigurable Computing

- Fast
- Inflexible

Reconfigurable Computing

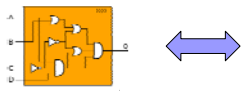
- No standard definition
- ***"Computing via a post-fabrication and spatially programmed connection of processing elements."***
  -John Wawrzynek Sp04
- A computer that can *RE*-configure itself to perform computation spatially as needed
  - How often do we *RE*-configure?
  - Coarse-grain? Fine-grain?
- Example: FPGA

Introduction to the FPGA

- Field Programmable Gate Array
- Began as ASIC replacements
  - ASIC that can be configured "in the field"
  - At power up, configuration is loaded onto the chip
  - Chip acts as an ASIC until power down
- Modern FPGA more like computers
  - Exploit *dynamic*, *partial* ***re***configuration
  - Embedded processors
- Xilinx, Altera are 2 major market leaders

The LUT

- LUT: ***L***ook***u***p ***T***able
- A direct implementation of a truth table
  - Recall a TT uniquely defines a circuit



A	B	C	D	Q
0	0	0	0	0
0	0	0	1	0
…				
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

- An n-LUT implements any n-input combinational logic
  - Depends on LUT configuration

Making a 2-LUT from Truth Table

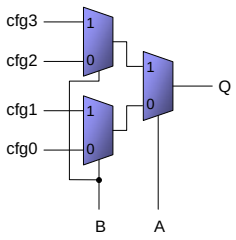
A	B	FALSE	AND	…	OR	…	NAND	TRUE
0	0	0	0		0		1	1
0	1	0	0	…	1	…	1	1
1	0	0	0		1		1	1
1	1	0	1		1		0	1

16 possible ways

4 configuration bits

2-LUT: CL and MUX Based

cfg3	cfg2	cfg1	cfg0	A	B	Q
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	0
0	0	0	1	0	1	0
			…			
1	1	1	1	1	0	1
1	1	1	1	1	1	1

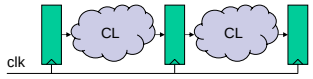


LUTs in Real Life

- 3-LUT and 4-LUT are most common
- SRAM based
- Learn, and use, them a lot in CS150

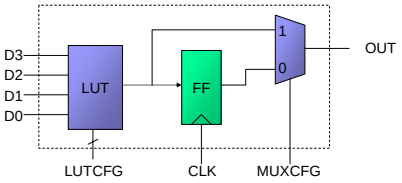
Sequential logic

- Connecting multiple LUTs gives us ***ANY*** combinational logic we want to implement
- We need Flip-Flop to build sequential circuits



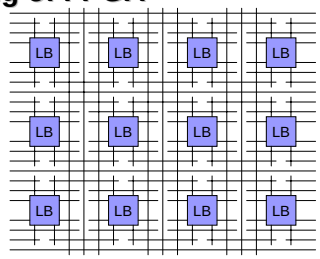
- FF are so important that they are included natively on FPGAs next to each LUT
- LUT + FF + … = LB (Logic Block)

Logic Block



- Can build any 4-input circuit
  - Synchronous OR Asynchronous
- Combining Logic Blocks => ANY synchronous digital circuit
- How to we build bigger circuit?

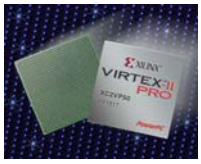
Routing of FPGA



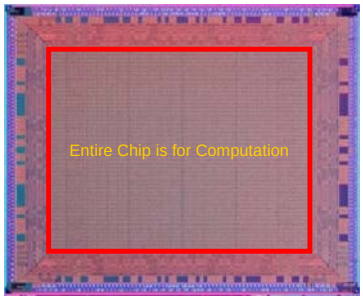
- With enough smartness in placement and routing, we can implement any synchronous digital circuits!

Example: Xilinx Virtex2pro xc2vp70

- 74,448 Logic Cells (LB)
- 2 PowerPC cores
- 328 18x18 bits multipliers
- 5904 Kbytes on chip memory
- 8 Digital Clock Managers
- 996 I/O pins
- 16 high speed serial I/O ports



Die Photo of a FPGA



Spartan-3 90nm CMOS

Real Stuff: BEE2

- Developed at Berkeley
  - Berkeley Wireless Research Center
- 5 Xilinx xc2vp70
- 40Gbytes DDR2 memory
- Used for research in:
  - Wireless
  - Astro-Physics (SETI)
  - Bioinformatics
  - Speech Recognition

Conclusion

- The Processor is NOT the only way to do computation
- Reconfigurable computers allows different tradeoffs among speed, flexibility, cost, power, etc
- FPGA offers fine-grain reconfigurability