1. Data Level Parallelism

The idea central to data level parallelism is vectorized calculation. Thanks to the Intel intrinsics (Intel proprietary technology), we can use specialized instructions to deal with multiple data with one instruction.

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>__m128i_mm_load1_si128( )</td>
<td>returns 128-bit one vector</td>
</tr>
<tr>
<td>__m128i_mm_loadu_si128( __m128i *p )</td>
<td>returns 128-bit vector stored at pointer p</td>
</tr>
<tr>
<td>__m128i_mm_mul_ps( __m128 a, __m128 b)</td>
<td>returns vector (a0<em>b0, a1</em>b1, a2<em>b2, a3</em>b3)</td>
</tr>
<tr>
<td>void_mm_storeu_si128( __m128i *p, __m128i a )</td>
<td>stores 128-bit vector a at pointer p</td>
</tr>
</tbody>
</table>

1. Implement the following function, which returns the sum of two arrays:

```c
static int product_naive(int n, int *a) {
    int product = 1;
    for (int i = 0; i < n; i++) {
        product *= a[i];
    }
    return product;
}

static int product_vectorized(int n, int *a) {
    int result[4];
    __m128i prod_v = __m128i(0);
    for (int i = 0; i < n; i += ____) { // Vectorised loop
        prod_v = __m128i(0);
    }
    __mm_storeu_si128(___________, __________);
    for (int i = ______; i < ______; i++) { // Handle tail case
        result[0] *= ______;
    }
    return ________________________________;
}
```
2. Thread Level Parallelism

As powerful as data level parallelization is, it provides rather inflexible functionalities. The use of thread is much more powerful and versatile in many areas of programming. And OpenMP provides the hassle-free, plug-and-play directives to use of threads. Some examples of OpenMP directives:

```c
#pragma omp parallelism
/* code here */
```

```c
#pragma omp parallel
for (int i = 0; i < n; i++)
/* code here */
```

1. For the following snippets of code below, circle one of the following to indicate what issue, if any, the code will experience. Then provide a short justification. Assume the default number of threads is greater than 1. Assume no thread will complete before another thread starts executing. Assume arr is an int array with length n.

a) // Set element i of arr to i
   #pragma omp parallel
   (int i = 0; i < n; i++)
   arr[i] = i;
   Sometimes incorrect
   Always incorrect
   Slower than serial
   Faster than serial

b) // Set arr to be an array of Fibonacci numbers.
   arr[0] = 0;
   arr[1] = 1;
   #pragma omp parallel for
   for (int i = 2; i < n; i++)
   arr[i] = arr[i-1] + arr[i - 2];
   Sometimes incorrect
   Always incorrect
   Slower than serial
   Faster than serial

c) // Set all elements in arr to 0;
   int i;
   #pragma omp parallel for
   for (i = 0; i < n; i++)
   arr[i] = 0;
   Sometimes incorrect
   Always incorrect
   Slower than serial
   Faster than serial

2. Consider the following code:
   // Decrements element i of arr. n is a multiple of omp_get_num_threads()
   #pragma omp parallel
   { int threadCount = omp_get_num_threads();
     int myThread = omp_get_thread_num();
     for (int i = 0; i < n; i++)
     { if (i % threadCount == myThread)
       arr[i] *= arr[i];
     }
   }
   What potential issue can arise from this code?
3. Data race and Atomic operations.

The benefits of multi-threading programming come only after you understand concurrency. Here are two most common concurrency issues:

- **Cache-incoherence**: each hardware thread has its own cache, hence data modified in one thread may not be immediately reflected in the other. The can often be solved by bypassing cache and writing directly to memory, i.e. using `volatile` keyword in many languages.
- The famous **Read-modify-write**: Read-modify-write is a very common pattern in programming. In the context of multi-thread programming, the interleaving of R,M,W stages often produces a lot of issues.

To solve problem with Read-modify-write, we have to rely on the idea of **undisrupted execution**.

In RISC-V, we have two categories of atomic instructions:

- Load-reserve, store-conditional (undisrupted execution across multiple instructions)
- Amo.swap (single, undisrupted memory operation) and other amo operations.

Both can be used to achieve atomic primitives, here are two examples.

### Test-and-set

<table>
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<tbody>
<tr>
<td><code>addi</code></td>
<td>t0 x0 1 #locked state is 1</td>
</tr>
<tr>
<td><code>amoswap.w.aq</code></td>
<td>t1 t0 (a0)</td>
</tr>
<tr>
<td><code>bne</code></td>
<td>t1 x0 start #if the lock is not free, retry</td>
</tr>
<tr>
<td><code>amoswap.w.rl</code></td>
<td>x0 x0 a0 #release lock</td>
</tr>
</tbody>
</table>

### Compare-and-swap

<table>
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<tr>
<td><code>lr</code></td>
<td>a3 (a0)</td>
</tr>
<tr>
<td><code>bne</code></td>
<td>a3 a1 fail #CAS fail</td>
</tr>
<tr>
<td><code>sc</code></td>
<td>a3 a2 (a0)</td>
</tr>
<tr>
<td><code>bnez</code></td>
<td>a3 start #retry if store failed</td>
</tr>
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<tr>
<td><code>amoswap.w.rl</code></td>
<td>x0 x0 a0</td>
</tr>
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Fail: #failed CAS

### Instruction definitions:

- **Load-reserve**: Loads the four bytes from memory at address x[rs1], writes them to x[rd], sign-extending the result, and registers a reservation on that memory word.
- **Store-conditional**: Stores the four bytes in register x[rs2] to memory at address x[rs1], provided there exists a load reservation on that memory address. Writes 0 to x[rd] if the store succeeded, or a nonzero error code otherwise.
- **Amoswap**: Atomically, let t be the value of the memory word at address x[rs1], then set that memory word to x[rs2]. Set x[rd] to the sign extension of t.

Question: why do we need special instructions for these operations? Why can't we use normal load and store for `lr` and `sc`? Why can't we expand amoswap to a normal load and store?