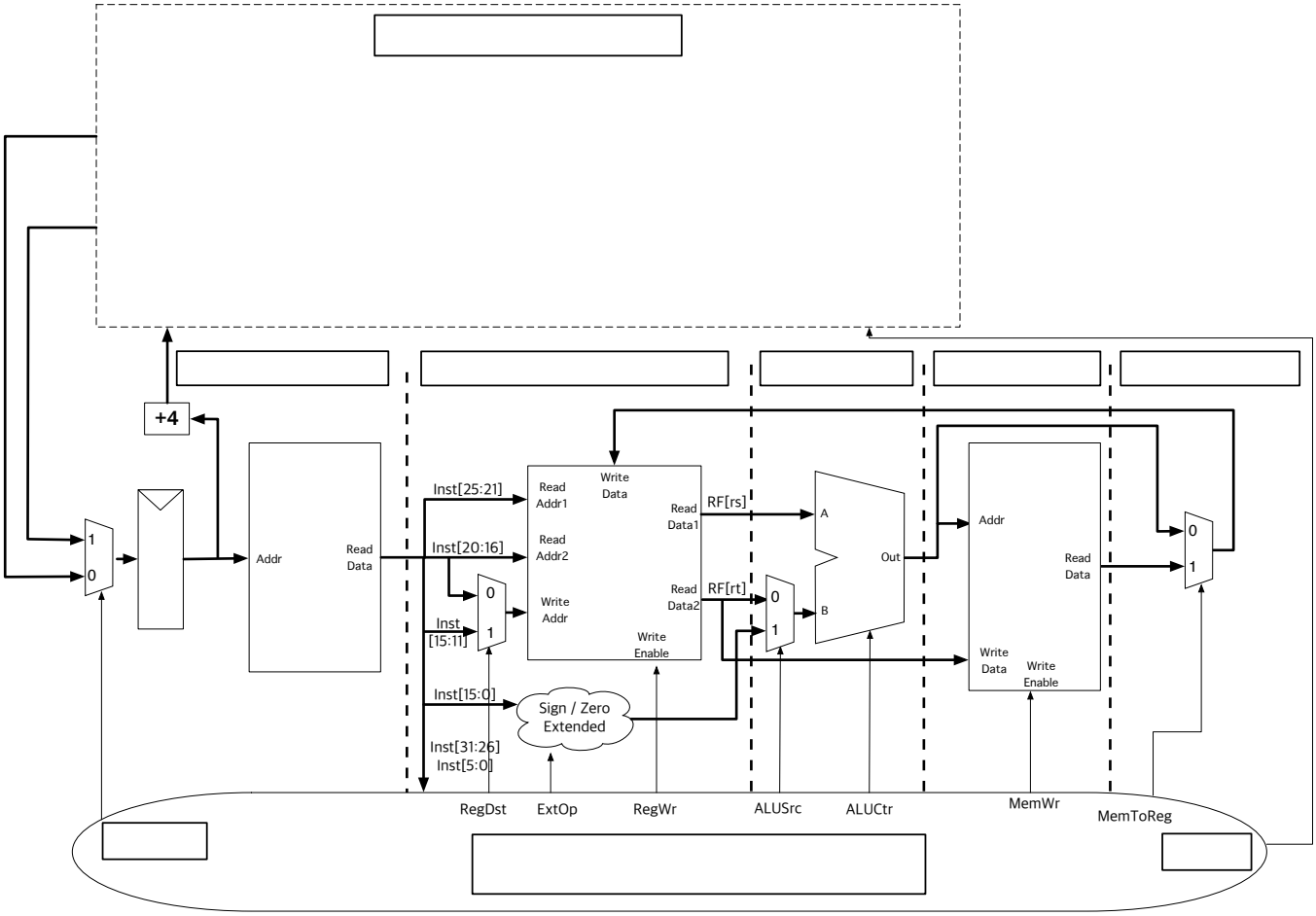
Single Cycle CPU Design

Here we have a single cycle CPU diagram. Answer the following questions:

1. Name each component.
2. Name each datapath stage and explain its functionality.

Stage	Functionality

3. Provide data inputs and control signals to the next PC logic.
4. Implement the next PC logic.



Single Cycle CPU Control Logic

Fill out the values for the control signals from the previous CPU diagram.

Instrs.	Control Signals								
			RegDst	ExtOp	ALUSrc	ALUCtr	MemWr	MemtoReg	RegWr
`add`									
`ori`									
`lw`									
`sw`									
`beq`									
`j`									

This table shows the ALUCtr values for each operation of the ALU:

Operation	AND	OR	ADD	SUB	SLT	NOR
ALUCtr	0000	0001	0010	0110	0111	1100

Clocking Methodology

- The input signal to each state element must stabilize before each rising edge.
- Critical path: Longest delay path between state elements in the circuit.
- $t_{clk} \geq t_{clk\text{-}to\text{-}q} + t_{CL} + t_{setup}$, where t_{CL} is the critical path in the combinational logic.
- If we place registers in the critical path, we can shorten the period by reducing the amount of logic between registers.

Single Cycle CPU Performance Analysis

The delays of circuit elements are given as follows:

Element	Register clk-to-q	Register Setup	MUX	ALU	Mem Read	Mem Write	RegFile Read	RegFile Setup
Parameter	$t_{clk\text{-}to\text{-}q}$	t_{setup}	t_{mux}	t_{ALU}	$t_{MEMread}$	$t_{MEMwrite}$	t_{RFread}	$T_{RFsetup}$
Delay(ps)	30	20	25	200	250	200	150	20

1. Give an instruction that exercises the critical path.

2. What is the critical path in the single cycle CPU?

3. What are the minimum clock cycle, $t_{clk,}$ and the maximum clock frequency, f_{clk}? Assume the $t_{clk\text{-}to\text{-}q}$ > hold time.

4. Why is a single cycle CPU inefficient?

5. How can you improve its performance? What is the purpose of pipelining?