8 Gb 3-D DDR3 DRAM Using Through-Silicon-Via Technology

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***Abstract*—An 8 Gb 4-stack 3-D DDR3 DRAM with through-Si-via is presented which overcomes the limits of conventional modules. A master-slave architecture is proposed which decreases the standby and active power by 50 and 25%, respectively. It also increases the I/O speed to $>$ 1600 Mb/s for 4 rank/module and 2 module/channel case since the master isolates all chip I/O loadings from the channel. Statistical analysis shows that the proposed TSV check and repair scheme can increase the assembly yield up to 98%. By providing extra VDD/VSS edge pads, power noise is reduced to $<$ 100 mV even if all 4 ranks are refreshed every clock cycle consecutively.**

***Index Terms*—Through-silicon-via (TSV), via last, via middle, via first, three dimensional, 3-D architecture, stack, master, slave, DDR3 DRAM, double data rate, rank, module, connectivity check and repair, assembly yield, power noise reduction, refresh, power edge pads, seamless, gapless read.**

I. Introduction

THROUGH-SILICON-VIA (TSV) has emerged as a promising solution in building 3-D stacked devices. It is a technology where vertical interconnects are formed through the wafer to enable communication among the stacked chips [1], [2]. There are also other wafer level processing technologies to form 3-D structures including the single-crystal Si layer stacking method [3], [4]. However, in such case, transistors get exposed to additional high-temperature heat cycles during fabrication, which can result in performance drift and variation. Also it puts limitations on the maximum number of layers that can be stacked. TSV, on the other hand, is more practical since it does not have such issues. This technology, however, faces other technical challenges which need to be overcome. These challenges include reliable wafer thinning process and high-yield die-to-die joining [1].

TSV technology is believed to have the potential to open up many new horizons in the semiconductor industry in the near future. This is because it provides many benefits including high density, high band-width, low-power, and small form-factor [5], [6]. Also, as we near the limit of technology scaling, it is believed to be a promising solution to overcome the scaling limit. CMOS image sensor with TSV is the first example where this technology was successfully commercialized. It went into production in 2008. Another possible application is "logic+memory" system-in-package (SIP), where a single or multiple memories are directly stacked on top of a logic chip [7], [8]. Here, the logic chip and the memory can communicate through thousands of IOs allowing high-bandwidth with low power. Also heterogeneous multi-level SIP, and 3-D logic chip applications are expected to emerge in the future. In the former application, TSVs are used to interconnect logic, memory, analog, RF sensor and MEMS chips among others. In the latter one, a logic chip itself such as CPU, can be built 3-dimensionally [9]. By proper floor-planning, interconnection lengths can be minimized, resulting in reduced delay and power. Other possible candidates are the high-density flash and DRAM. In flash memories, TSVs are considered primarily because they enable smaller package size. In DRAMs, on the other hand, there is much interest in TSVs since they can be used to improve performance and reduce power consumption, as will be described in this paper.

Demands for high-density and low-power continue to increase, especially in server applications. Currently, in order to increase the module density, more DRAM chips are simply added. However, this results in increased power waste due to duplication of circuit components.

DRAMs in modules are preferably arranged in multiple ranks to increase system band-width. However, this limits the input/output (I/O) speed since increased channel loading causes degradation in signal integrity.

To overcome the I/O speed limit, several buffered module solutions have been proposed, where data pins are buffered by additional chips. However, this increases power consumption and latency, significantly.

In this paper, a new 3-D DRAM with TSVs is proposed which overcomes the limits of conventional module approaches. Section II provides some general information on TSV fabrication technologies. Section III describes how the architecture and datapaths were designed. Section IV presents key 3-D technologies including TSV connectivity check and repair scheme, and power noise reduction method. Section V shows measurement results. Finally, a summary is given in Section VI.

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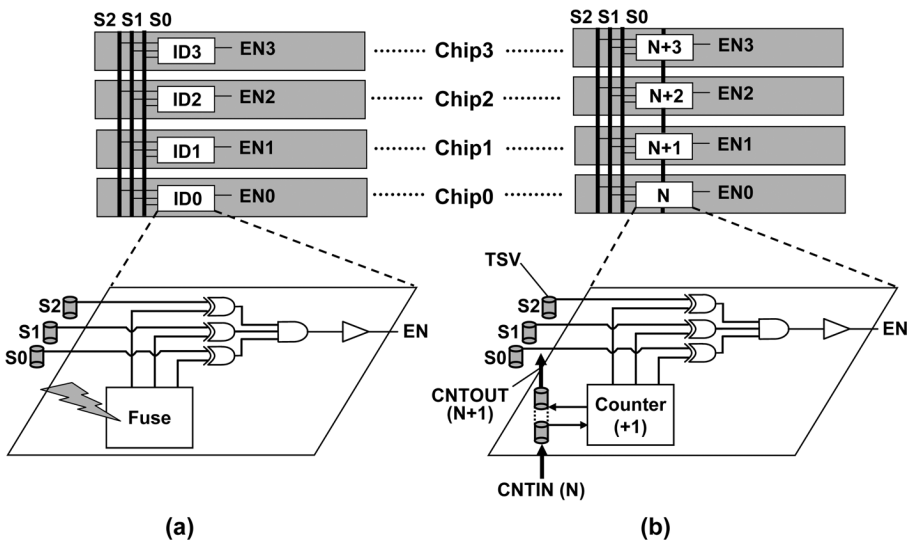

Fig. 1. Chip identification. (a) Fusing method. (b) Counter method.

II. TSV Fabrication

Based on at which process step the TSV is formed, the fabrication method can be classified into via-last, via-middle, and via-first processes [10], [11]. Here, vias are formed after the final process step, before metallization, and at the initial process step, respectively.

In the via-last process, metals such as W and Cu can be used as the filling material allowing to form high-conductivity interconnects. Also, TSVs can be formed simply after fab-out so that no special process integration during the normal process flow is required. In the via-first and via-middle processes, on the other hand, metal lines can run over the TSVs making routings more efficient. Also, chip identification (ID) can be done more efficiently after assembly during power-up. The via-first process uses polysilicon as the TSV filling material, increasing the resistance (typically up to 5 Ohms/TSV), which can cause problems with power delivery and increased propagation delay [12]. Via-last was adopted in this device, since it enables fabrication of high conductivity TSVs with a simpler process.

Chip identification (ID) is an important part of memory stacking since it affects the entire assembly flow. In order to distinguish identical chips, a unique ID is provided to each stack. It is compared against the selection signal sent from the controller to enable a chip if there is a match. Typically, fusing and counter methods are used as shown in Fig. 1. In the former method, chip ID is provided to each stack through laser fusing before assembly. In the latter method, chip ID is automatically assigned by counters connected in a serial chain, during power-up after all chips are fully assembled and packaged.

Even though the counter method is more desirable, the fusing method was used in this device. This is because the counter method cannot be applied to the via-last process since a vertical serial path cannot be formed.

III. 3D-TSV DRAM

A. Device Architecture

A new 3-D architecture was developed in order to improve the performance and to reduce power consumption compared to the conventional quad-die packages (QDPs). In the QDP, 4 normal DRAMs are simply stacked and wire-bonded to the package. In the 3D-DRAM, a single master chip is located at the bottom and three slave chips are stacked on top as shown in Fig. 2. All chips are assembled face down in a flip-chip package. They are connected through around 300 TSVs and each stack constitutes a rank. While the device which consists of an interface chip and multiple core chips is configured in a single rank [12], the 3-D DRAM supports 4-rank module functions. Conceptually, the master is a normal DRAM with additional multi-rank control circuitry and datapath. The slave, on the other hand, has simply a memory core and wafer level test circuitry.

Table I summarizes important specifications of the 3-D DRAM. Each DRAM is 2 Gb resulting in a total device density of 8 Gb. The interface is fully compatible with the DDR3 industry standard. The maximum data rate is 1600 Mb/s and the read latency is 10 cycles at 1333 Mb/s. The I/O organization is X4. Eighteen packages in total including two packages for error-correction-code (ECC) can be assembled to build a 16 GB module.

This architecture, as shown in Fig. 3, allows high I/O data rate since the master acts as a buffer which isolates the channel and the slave chips. The I/O data rate is increased to 1600 Mb/s, while it is limited to 1066 Mb/s in conventional quad-die package (QDP) structures (4 ranks/module, 2 modules/channel case).

In this structure, power is reduced compared to the QDPs since redundant circuits including delay-locked-loop (DLL), input buffers, and clock circuitry are eliminated in the slaves. If 4 ranks are in stand-by (IDD2N) and active (IDD1) states, power is expected to be reduced by 50 and 25%, respectively.

One drawback of the 3-D architecture compared to the QDPs is that the read latency is increased. This is because both the read command signal and data see TSV loadings ($\sim$300 fF/TSV) resulting in increased overall propagation delay. Simulation results show that the latency is increased by 1 clock cycle at 1333 Mb/s. This increase, however, is small compared to the 3–4 cycles added in other buffered module solutions.

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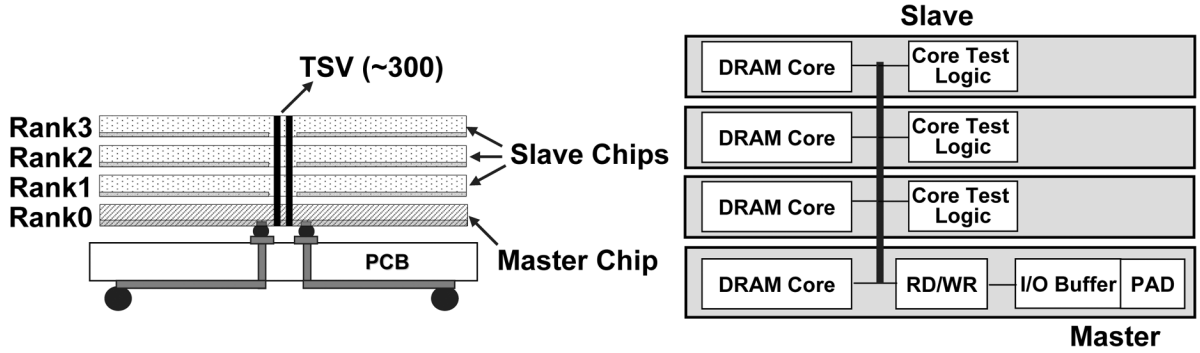

Fig. 2. 3D-TSV DRAM cross-sectional view and conceptual drawing.

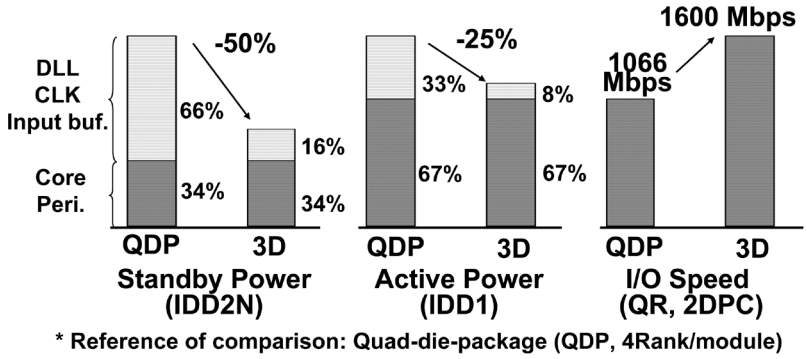

Fig. 3. Advantages of the 3D-TSV DRAM architecture.

TABLE I
SUMMARY OF 3-D DRAM SPECIFICATIONS

Items	Spec
Type	DDR3
VDD	1.5V
Density (Mono)	2Gb
Density (Stack)	8Gb [2Gb * 4]
Data rate	1600Mbps
CL	10 cycles
Organization	X4

	3D TSV module	Buffered DIMM
*Standby-power (IDD2N)	48%	100%
*Active power (IDD1)	65%	100%
Latency @1333Mbps	1 cycle	3~4 cycles
Cost adder	TSV process cost	2 buffer cost
Density	Max 4 rank	
Speed@2DPC	~ 1600Mbps (QR X4)	

*3D module PLL+register: ~2W, Buffered-DIMM 2 buffer chips: ~4.3W

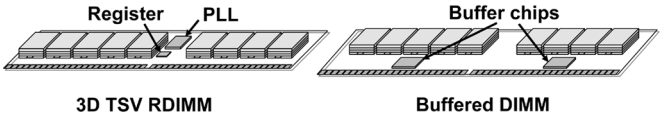

Fig. 4. Advantages of the 3D-TSV RDIMM over buffered DIMM.

Several buffered modules have been proposed to achieve high IO speed. Command, address, and DQs are buffered with one or two additional buffer chips, which add power consumption, latency, and cost. In Fig. 4, the registered dual-inline memory module (RDIMM) with 3-D DRAMs and the buffered module with two buffer chips are compared. The standby power and active power of the 3-D module are only 48% and 65% of those of the buffered module, respectively. This is because, 3-D DRAMs and PLL+register chip consume less power than normal quad-die-packages (QDPs) and the two buffer chips, respectively (assumed PLL+register chip: 2 W; two buffer chips: 4.3 W). Latency overhead due to the buffer chip in the buffered DIMM is 3 to 4 cycles at 1333 Mb/s as compared to 1 cycle in the 3-D RDIMM. Whether the 3-D DIMM wins in cost or not depends on whether the TSV process cost can be less than the two additional buffer cost. Achievable maximum IO speed is expected to be comparable.

B. Datapath Structure

A datapath optimized for 3-D architecture was developed. Two key factors in the datapath design were that internal reads and writes among ranks through TSVs can occur simultaneously and that process-voltage-temperature (PVT) variations can exist among different chips. Fig. 5 shows the entire datapath for the master and slave chips. The datapath consists of what is called the local and global datapaths. The local datapath is controlled locally when the corresponding chip is selected. On the other hand, the global datapath is accessed and controlled when any

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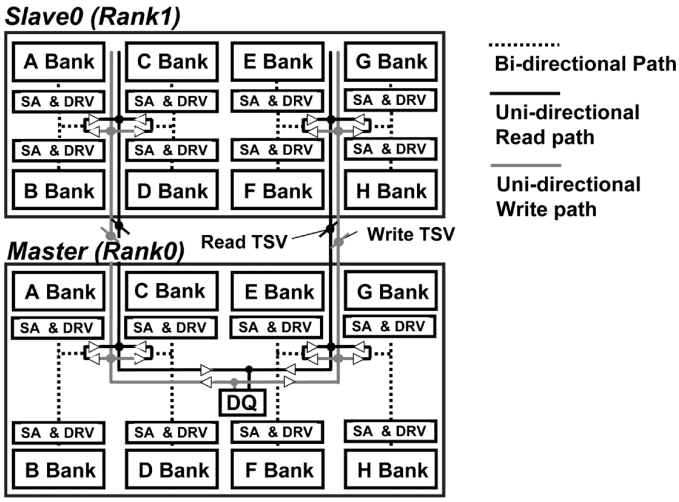

Fig. 5. Master-slave chip datapath structure.

of the stacked chips is selected. The local datapath is bidirectional (read/write shared) while the global datapath is uni-directional (read/write separated). The global datapath is separated for reads and writes since internal reads and writes can occur simultaneously, when a write to a rank is followed by a read to another rank. Write and read TSVs are also allocated separately since they are also parts of the global datapath.

Despite area penalties, separate data TSV sets are allocated for left (A/B/C/D) and right bank groups (E/F/G/H), in order to make signal and data lines travel less on the local path. This makes the 3-D chip less dependent on different PVT conditions of each die. Depending on whether 1 or 2 TSV sets are allocated, all signals would travel about half or quarter of the chip width in the slaves, respectively.

IV. 3D-TSV Design Technologies

A. TSV Connectivity Check and Repair Scheme

Decreasing the TSV cost is a crucial factor in the successful commercialization of this technology. Increasing the assembly yield is one of the most critical factor in total cost reduction. Even though it is desirable that the TSV process itself provide assembly yield of up to $>98\%$, there may be some limitations in getting to this point due to many technical challenges. Even if technical challenges are overcome in the future, it may take some time until this yield level is achieved. Circuit techniques can be applied in order to assist to increase the assembly yield. Depending on the TSV process maturity, it is believed that these techniques can be either an interim solution or a mandatory one in the future.

A TSV connectivity check and repair scheme was developed to increase the assembly yield. First an open-short test is conducted between the chips externally whereby the failed TSVs are identified. The open-short info of each TSV is stored in a latch located next to each TSV. All latches are connected serially and the stored data is clocked out through the scan chain. By analyzing the scanned-out data, the corresponding addresses of the failed TSV locations are identified. All failed TSVs are repaired by programming the corresponding e-fuses.

TABLE II
Estimated TSV Yield for Different Signal to Redundant TSV Ratios for 4 and 8 Chip Stacks With 300 TSVs

Signal TSV # : Redundant TSV #	Assembly yield [%] (300 TSVs)	
	4 Stacks	8 Stacks
2:1	95	76
4:2	99.8	98

A TSV repair scheme shown in Fig. 6 was developed. In general, certain number of redundant TSVs is allocated to a group of TSVs. Redundancy is needed for all command, address and DQ related signals. If one of the actual TSVs fails, it is replaced by one of the redundant TSVs. In the conventional structure, those redundant TSVs are dedicated and fixed in location. In the proposed scheme, however, there is no distinction between the actual and redundant TSVs. If a failure occurs at a TSV, the remaining TSVs are all shifted to the neighboring ones, whereby it is guaranteed that a failed TSV is always repaired with a neighboring TSV. This decreases the detour path, reduces routing complexity and loadings.

In order to determine the proper TSV signal to redundancy ratio and to estimate the yield gain, a statistical analysis has been performed, considering trade-offs between yield improvement and chip area penalty. Based on the current yield data for a 2 chip stacked device with 100 TSV interconnections, the failure probability of a single TSV was first derived. This failure rate has been used to estimate the assembly yield for 4 to 8 chip stacks with 300 signal TSVs. The TSV yield without any redundancy for 4 chip stacks has been calculated as 15%. Then this analysis has been extended to derive the yield for different signal to redundant TSV ratios. In this analysis, it has been assumed that each failure event is independent and occurs at random. However, if TSV failure occurs in grouped localized form, the above analysis would not be valid. In such case, for the repair scheme to be effective, the number of signal TSVs in a group would have to be increased.

Two additional redundant TSVs for a 4 signal TSV group has been selected as the first choice. Analytical results show that it provides an assembly yield of $>98\%$ for 4 stacked chips with 300 signal TSVs as shown in Table II. It is interesting to note that the 4:2 group has higher yield than the 2:1 group even though the total physical number of TSVs is the same in both cases. This is because the 4:2 group has more repair flexibility and there are less number of such groups. The chip size overhead due to the redundant TSVs mainly depends on the TSV pitch. Chip size overhead of $\sim 2\%$ is expected with 80 um TSV pitch.

B. VDD/VSS Noise Reduction Scheme

When a device pulls large amounts of current at once, VDD and GND bounces can occur which can result in functional failures. The noise peak is determined by the combined effect of current variation rate within the given time (di/dt), package inductance (L) and current-resistance (IR) voltage drop. The power noise is of a bigger concern in the 3D-DRAM than in a single DRAM since it has multiple ranks which can be operative almost at the same time. In order to estimate the power

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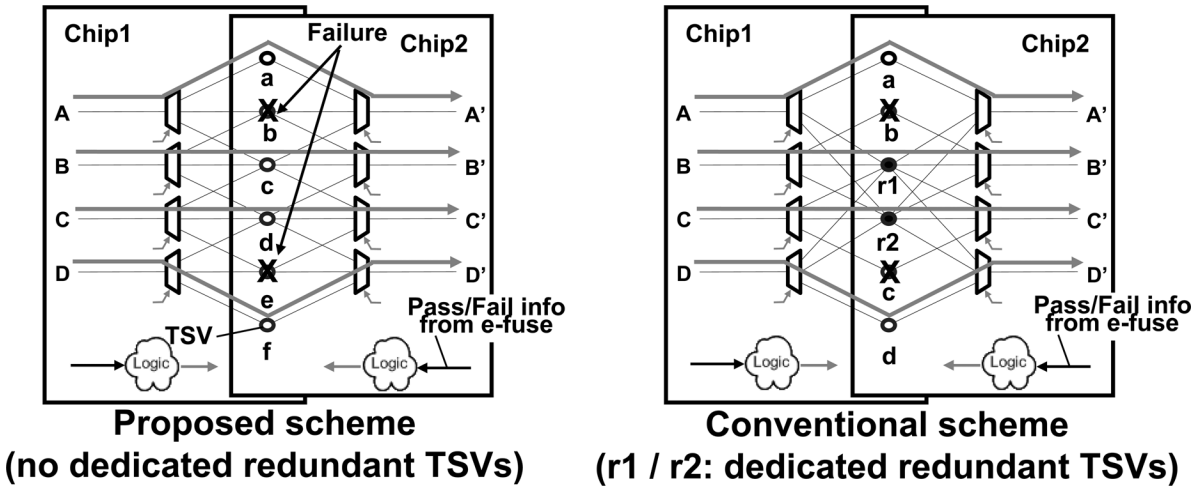

Fig. 6. Proposed TSV connectivity check and repair scheme.

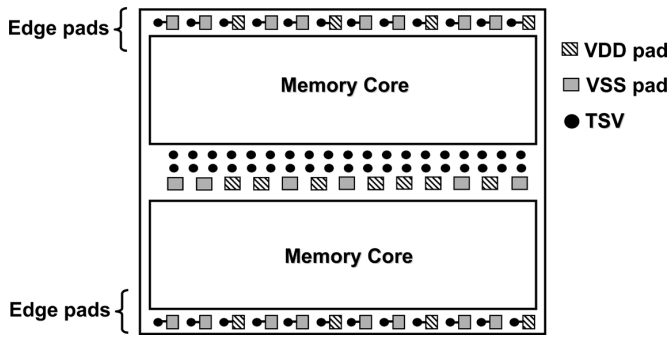

Fig. 7. 3-D power noise reduction scheme with VDD/VSS edge pads.

noise effect, all power lines were modeled in 3-D grids and full chip simulation was conducted.

In general, the largest VDD/VSS noise occurs in refresh modes. In field operations, the worst case power noise scenario is when all ranks are refreshed every clock cycle consecutively. In this case, total of 32 banks (8 banks per rank) are activated within 4 cycles which can result in functional failures. In order to overcome this problem, extra VDD/VSS pads and TSVs were added at the top and bottom edges of the chip, as shown in Fig. 7. 10 VSS and 5 VDD pads have been allocated per bank. Each edge pad is connected to a neighboring edge TSV. In the master chip, power is supplied through the edge pads which are attached to the package through solder bumps. In the slave chips, on the other hand, power is supplied through the edge TSVs.

Fig. 8 shows bit line sensing simulation results on VSS noise when all 4 ranks with 1 KB page sizes are refreshed every clock cycle consecutively. This figure shows noise signatures for 3 cases at the worst case location. In the first case, power is supplied through center pads and TSVs only (worst case location: top outer chip edge). In the second case, extra VDD/VSS TSV are placed at the top and bottom edges (worst case location: top outer chip edge). In the third case, besides extra VDD/VSS TSVs, extra edge power pads are also provided in the master chip (worst case location: top quarter chip). Fig. 8 shows that the ground noise is as high as 350 mV when TSVs are placed only at the center, while with power edge pads, the ground noise is reduced to about 100 mV. This is similar to the worst-case power noise of conventional DRAMs. VDD, on the other hand, is not as much affected by power noise due to the presence of internal power regulators. The chip size overhead due to the additional power TSVs is 0.5%.

TABLE III
PERFORMANCE IMPROVEMENT SUMMARY

	This work	Current solutions	Ref. of comparison
Standby-power (IDD2N)	50%	100%	QDP (4Rank/module)
Active-power (IDD1)	75%	100%	QDP (4Rank/module)
IO speed	>1600Mbps	1066Mbps	QDP (4Rank/module)
Latency	1 clock cycle	3~4 clock cycles	Buffered DIMM
Assembly yield	>98%	~15%	With and without TSV repair scheme
Power noise	<100mV	~350mV	With and without power enforcement

V. MEASUREMENT RESULTS

Fig. 9 shows the chip micrograph of the fabricated chip. 50 nm node DRAM process was used. The chip size is 10.9 mm $\times$ 9.0 mm. The master and slave dies are distinguished by a single metal layer. Arrays of $\sim$400 TSVs (signal and redundant TSVs total) are visible at the center of the die, and the edge VDD/VSS pads and TSVs are visible at the top and bottom. A micrograph of the cross section of the 4-stack 3-D DRAM is also shown. The TSV pitch and diameter are 80 um and 30 um, respectively. Table III summarizes important performance improvement results.

Fig. 10 shows measurement results on seamless rank-interleaved reads between 2 ranks at 1333 Mb/s, 1.5 V, room temperature. This is a unique feature of the fabricated device, which can potentially contribute to overall system performance improvement. In the conventional DDR3 system, if data is read through rank-interleaving, read-preamble requirement

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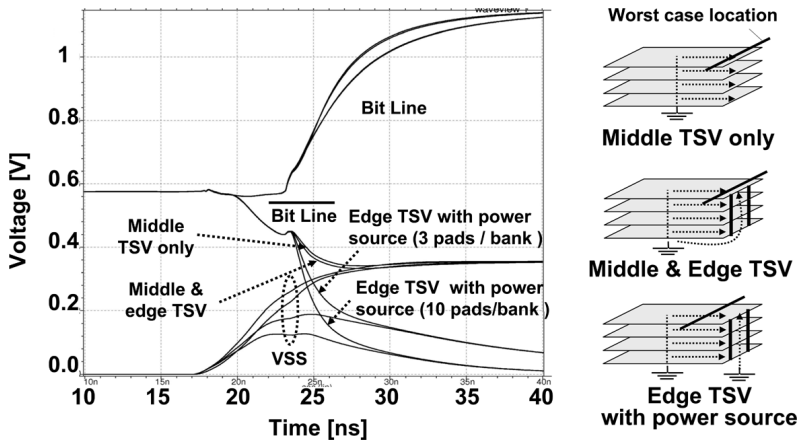

Fig. 8. Simulation results on bit line sense amp operation with power noise, when all 4 ranks are refreshed consecutively every clock cycle.

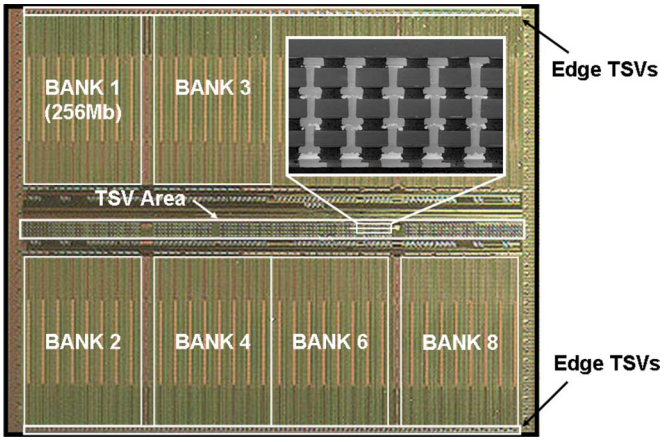

Fig. 9. Chip micrograph of the fabricated chip and cross-sectional view of TSVs. Chip size is 10.9 mm × 9.0 mm.

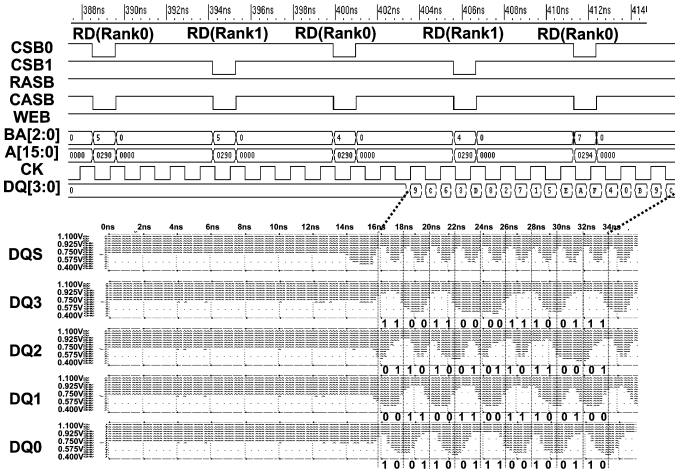

Fig. 10. Measurement results on seamless rank interleaved reads (1333 Mb/s, 1.5 V, room temp, $\mathrm{WL} = 7, \mathrm{BL} = 8, \mathrm{RL} = 10$).

causes 1 cycle data bubble to occur. In the 3-D chip, however, since only the master has control of the shared data bus, the pre-amble between reads is not required any more. This is an example showing that the device successfully supports module functions.

Fig. 11 shows the measured schmoo plot of the slave chip under the Xmarch condition at room temperature. The command and data patterns are as follows:

$$\begin{aligned}&\mathrm{Loop}(\mathrm{ACT} - \mathrm{WR\_D1} - \mathrm{PRE})\\&\quad => \mathrm{loop}(\mathrm{ACT} - \mathrm{RD\_D1} - \mathrm{WR\_D0} - \mathrm{PRE})\\&\quad => \mathrm{loop}(\mathrm{ACT} - \mathrm{RD\_D0} - \mathrm{WR\_D1} - \mathrm{PRE})\\&\quad => \mathrm{loop}(\mathrm{ACT} - \mathrm{RD\_D1} - \mathrm{PRE})\end{aligned}$$

where ACT, WR_D1, WR_D0, RD_D1, RD_D0, PRE denote activate, write data1, write data0, read data1, read data0, and precharge, respectively. Loop() denotes repeating the command sequence in parenthesis through the entire cells within the memory array. The timing relationship between ACT-WR/RD, PRE-ACT, WR-PRE, RD-PRE, RD-WR are tRCD, tRP, tRDL, tRTP, tRTW, respectively. In the measurement, they have been set to 10, 10, 21, 16, 10 clock cycles, respectively.

Fig. 12 shows measurement results on TSV connectivity check and repair scheme. First, a TSV failure map was obtained after performing the TSV connectivity check test. "F" and "P" denote failed and passed TSVs, respectively. For the sake of convenience, only a small part of the entire TSV array is shown. In this particular sample, "CASB" and "WEB" command TSVs did not get connected, so that the selected slave chip did not respond to any given commands. In order to confirm the effectiveness of the TSV repair scheme, the amount of current change during interleaved refresh (ICC5) operation was measured before and after the repair. For the repair, the e-fuses corresponding to the failed addresses were blown. As shown in Fig. 12, the refresh current increased by a factor of 1.8 after the repair, which shows that the failed TSVs were successfully repaired. By using the connectivity check and repair scheme, a mal-functional device was successfully repaired which would otherwise have to be discarded.

VI. Summary

A new 3-D DDR3 DRAM with TSVs was developed to overcome the limits of conventional modules. A master and slave

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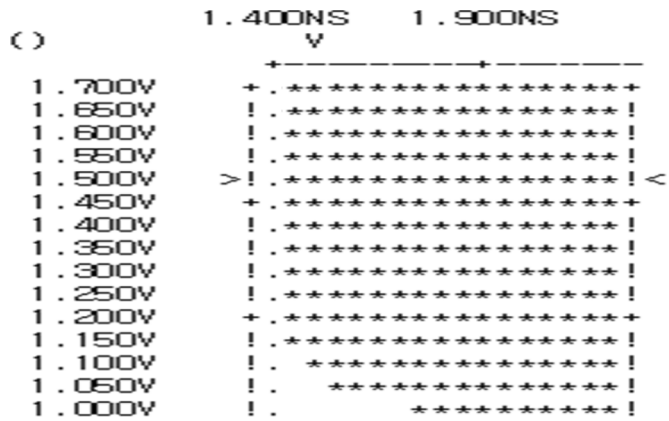

Fig. 11. Measured schmoo plot of the slave chip under the Xmarch pattern condition at room temperature.

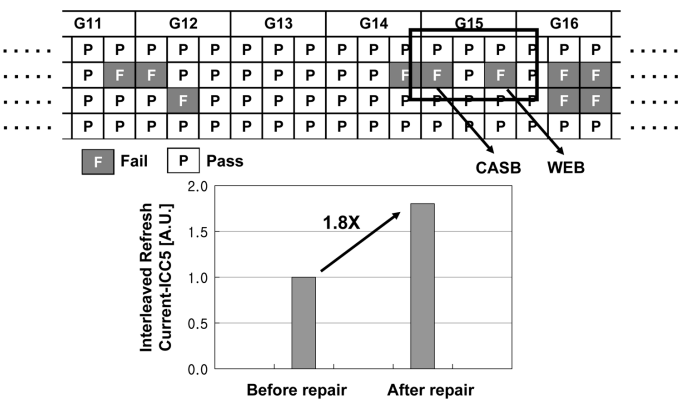

Fig. 12. TSV connectivity check and repair measurement results.

architecture has been proposed whereby the standby and active power is decreased by 50 and 25%, respectively, compared to the conventional QDPs. Also the IO speed is increased to 1600 Mb/s for 4-rank, 2 DIMM/channel case, since the master isolates the rest of the chip loadings from the channel. A TSV connectivity check and repair scheme was introduced to improve the assembly yield to a theoretical value of up to 98%. An edge power enforcement scheme was applied to reduce the VDD/GND noise when all 4 ranks are refreshed almost simultaneously. Functional 3D-DRAM samples were obtained and the effectiveness of the TSV connectivity check and repair scheme was demonstrated through measurements. The 3D-TSV module is a promising solution due to its low-power, high-speed, high-density, and low latency advantages over other existing modules.

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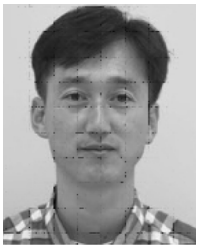

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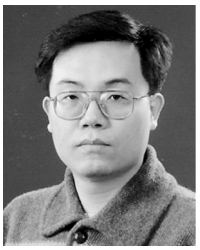

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Dr. Kim received the Grand Prize from the Samsung group for the successful development of 1 Mb and 1 Gb DRAMs in 1986 and 1996, respectively. He received several technical achievement awards from the R&D Center of Samsung for his work on the development of high speed devices and the characterization of submicron devices and reliability issues in high-density DRAMs, including reducing soft-error rates and reducing sensitivity to electrostatic discharge problems. He received the first prize for design excellence in student VLSI design contests at the Center for Integrated Sensors and Circuits in 1991 and 1993, sponsored by several U.S. companies. He serves as a committee member of the Symposium on VLSI Circuits and the A-SSCC. He was elected as an honorary Samsung Fellow in November 2004.

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