IIT Video Controller/Processor

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CS 294.48

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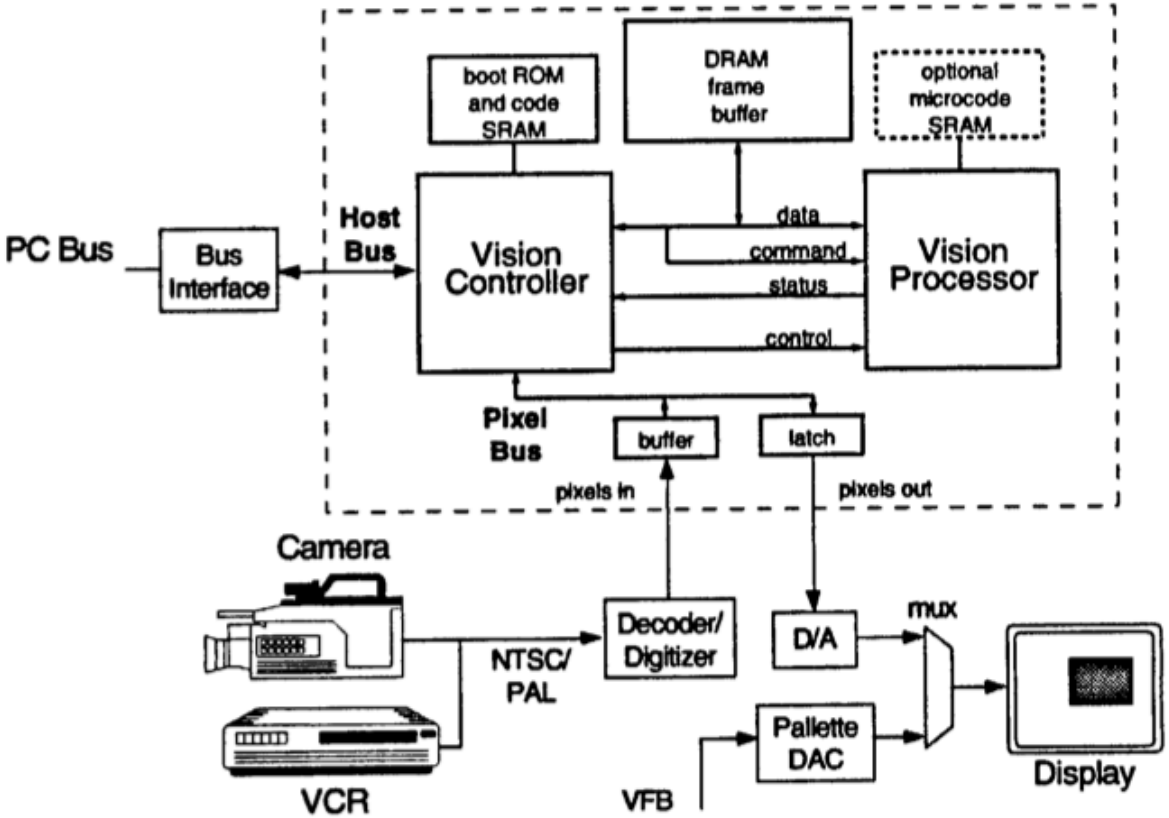
IIT Video Controller/Processor

- ca. 1992 ASIC pair for a PC's video interface
  - H.261/MPEG encoding/decoding
  - Digital video capture/output
    - A2D/D2A on separate chip
  - Programmable
  - Still present in low-end DVD players

System Architecture

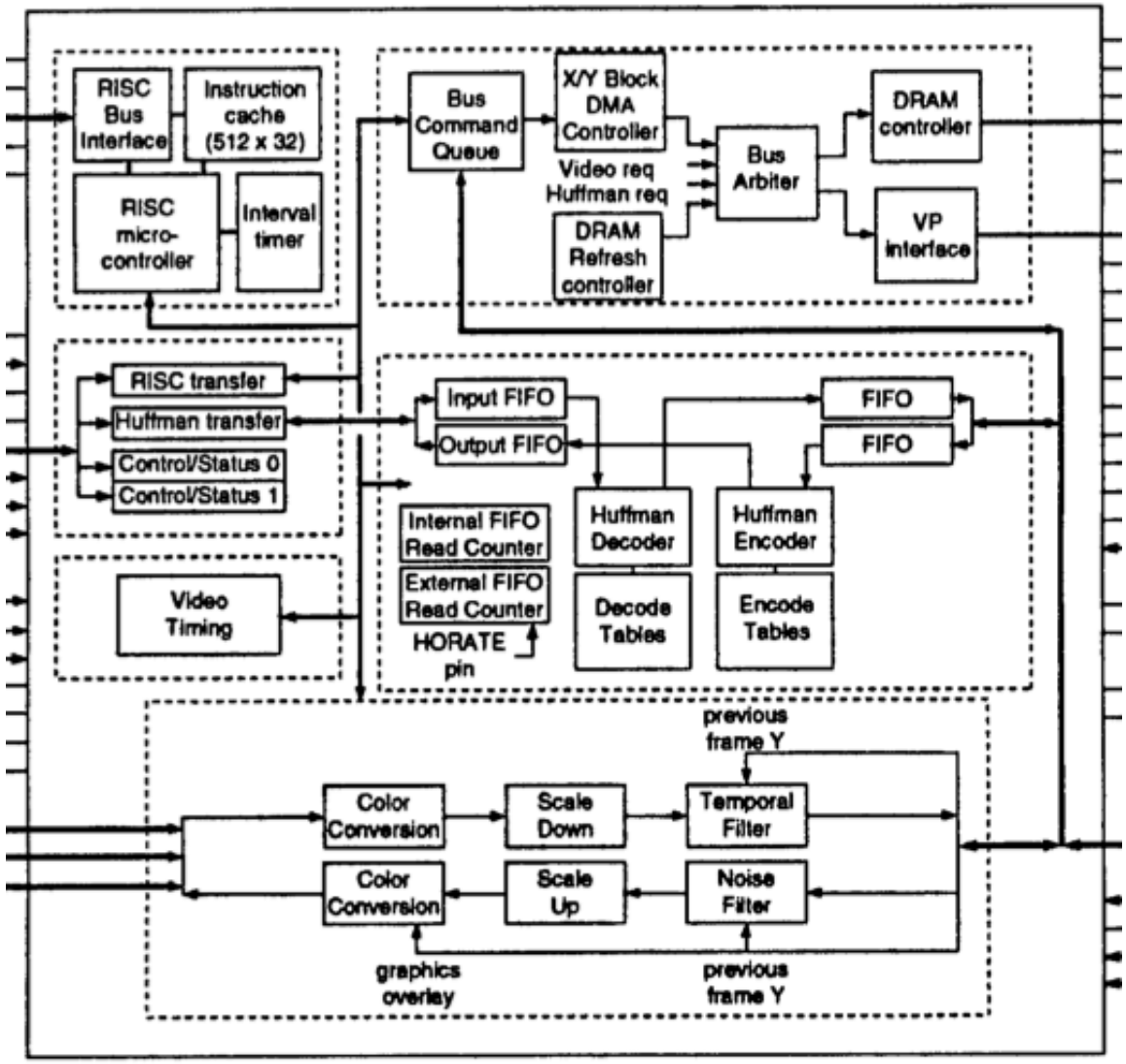


Vision Controller

MIPS-X
RISC core

Host IF

Pre/Post
Processing



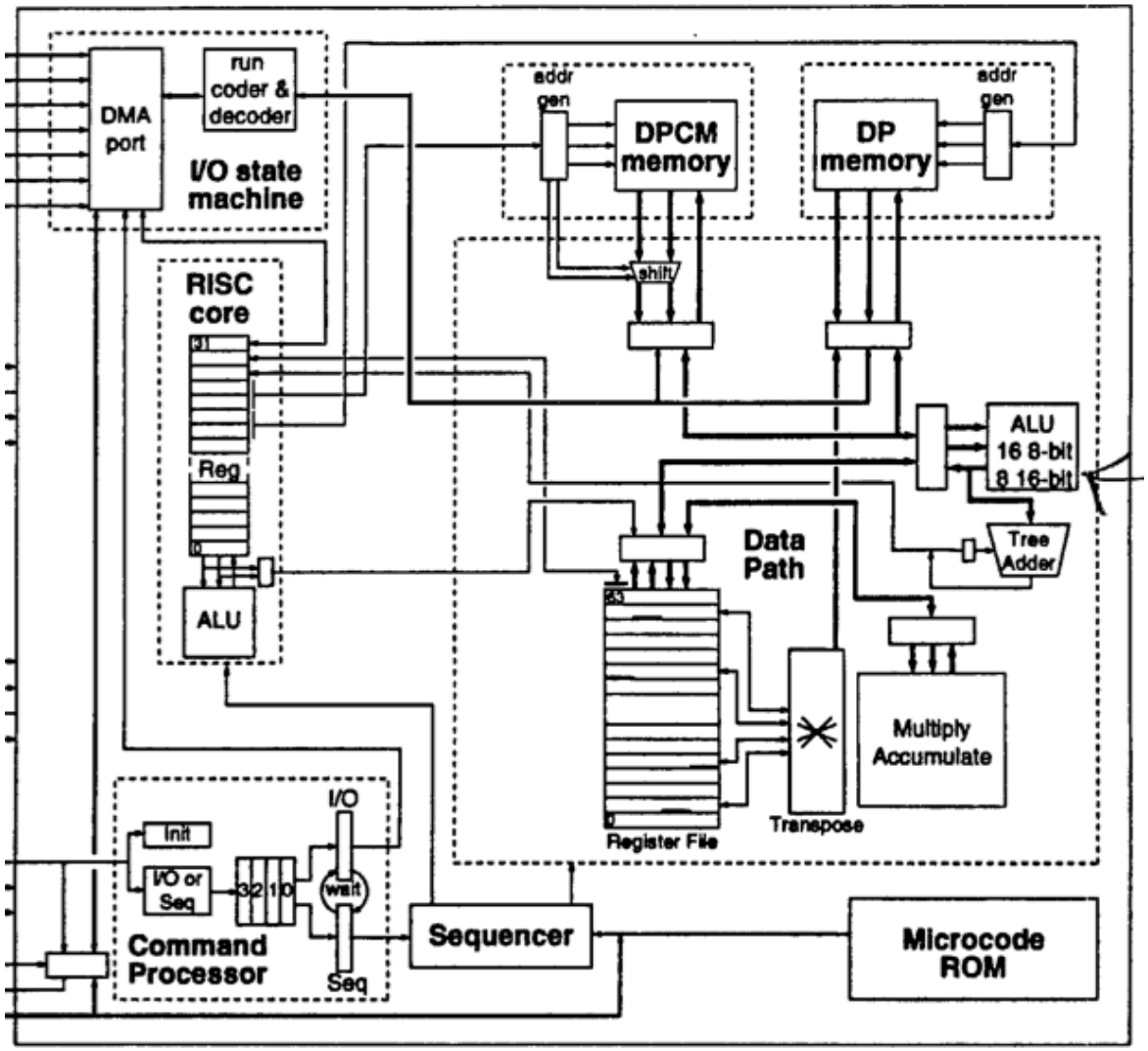
DMA
Engine

Huffman
Enc/Dec

Vision Processor

DMA Engine

RISC Core



Local Store

SIMD Datapath

Evident Patterns

- Heterogeneous MIMD shared memory
  - Nested SIMD in VP
- In-order pipelines
- Interconnnects are all buses or point-to-point
- Local stores, rather than caches