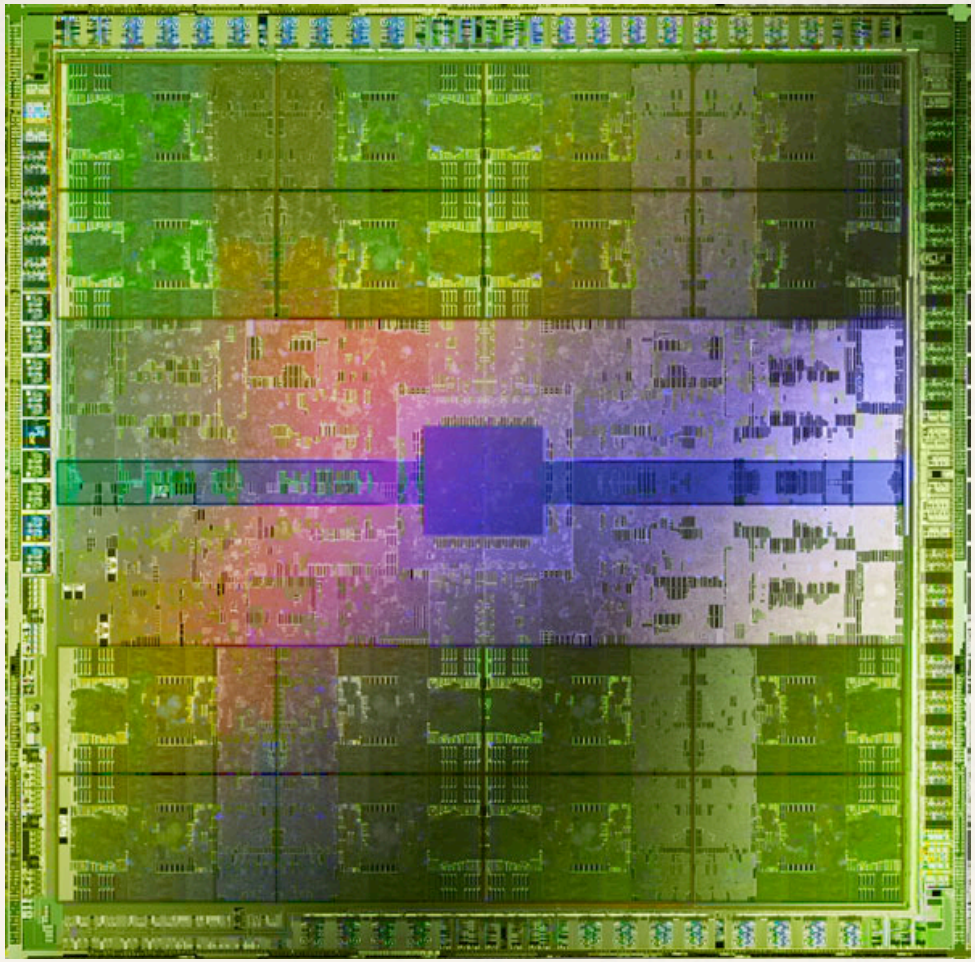


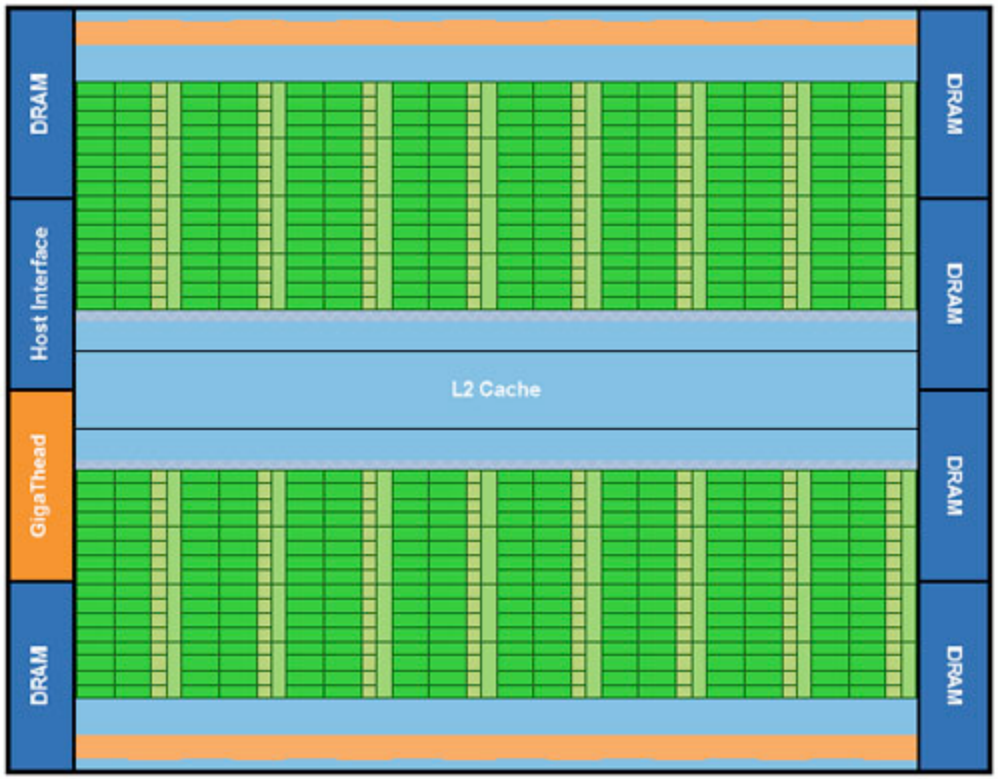
Image Courtesy www.nvidia.com

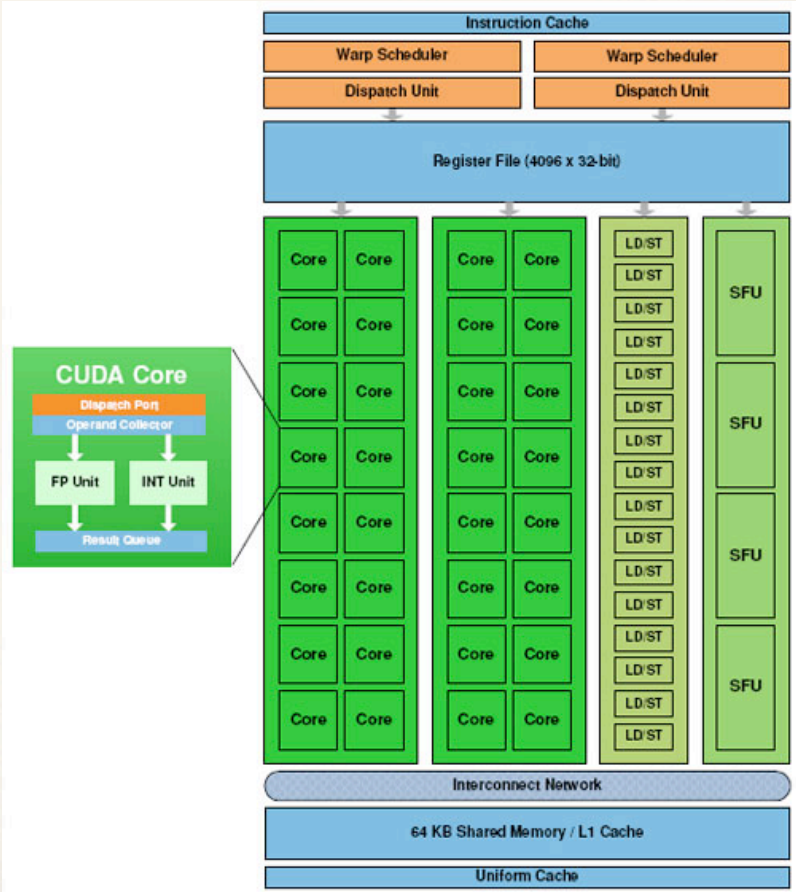
CS250 Section 6

Yunsup Lee

10/2/09

NVIDIA Fermi





Upcoming dates

- Lab 3 is due on October 6th (Tuesday) before class
  - You don't have separate late days for lab 3!
- Project proposal is due on October 8th (Thursday) before class
  - If you don't have a project partner or don't have a project topic talk with me after this section

CS301 stuff

- Being a TA at Berkeley for the first time, I need to take CS301
- Please fill in the survey
  - http://www.surveymonkey.com/s.aspx?sm=_2fIbwwtVr8X2jtqy9hpAxYQ_3d_3d
- Today's section will be recorded
- Thanks for your cooperation!

Project Proposals

- Take a look at Lecture 6: Infinicore
  - Due October 8
  - Title
  - Team members
  - 2-page PDF description of what you want to do
  - Where you will get functional model, test infrastructure
  - Initial guess at high-level block diagram
  - What does the design space look like and how you will explore it

Lab sections from now on

- Starting from next week's, lab section is turning into office hours
- That makes two hours of office hours
- I will be waiting for you in my office (577C aka ParLab)
- Then we will move to 611 (6th floor alcove)
- So first find me in the ParLab, and then 611

Tutorial 8: SRAM32x512

- Did you notice that there are two modes for power analysis?
  - Averaged mode
  - Time-based mode
- Power Analysis tool (PrimeTime PX) will fail on time-based analysis
  - Only vcdplus.power.avg.max.report will come out
- Max and min reports look the same
  - The makefiles are modified to only do max analysis

Lab 3: SRAM32x1024

- Place and Route during project v-sram32x1024 will take a long time
  - It is trying to fix DRC errors
  - The initial place is too tight so the tool is bouncing
  - You can fix it by doing pre-placing

Lab 3: Power Analysis

- The metric for Energy/Instruction is the average of the assembly tests
- You don't need to do time-based analysis for the C benchmarks

- Analytic model
  - You need to come up with an equation. For example,
    - Energy = sum_<type of instruction> <# of inst>*<Energy/inst>
  - TA will run a benchmark on your processor and plug it into your model

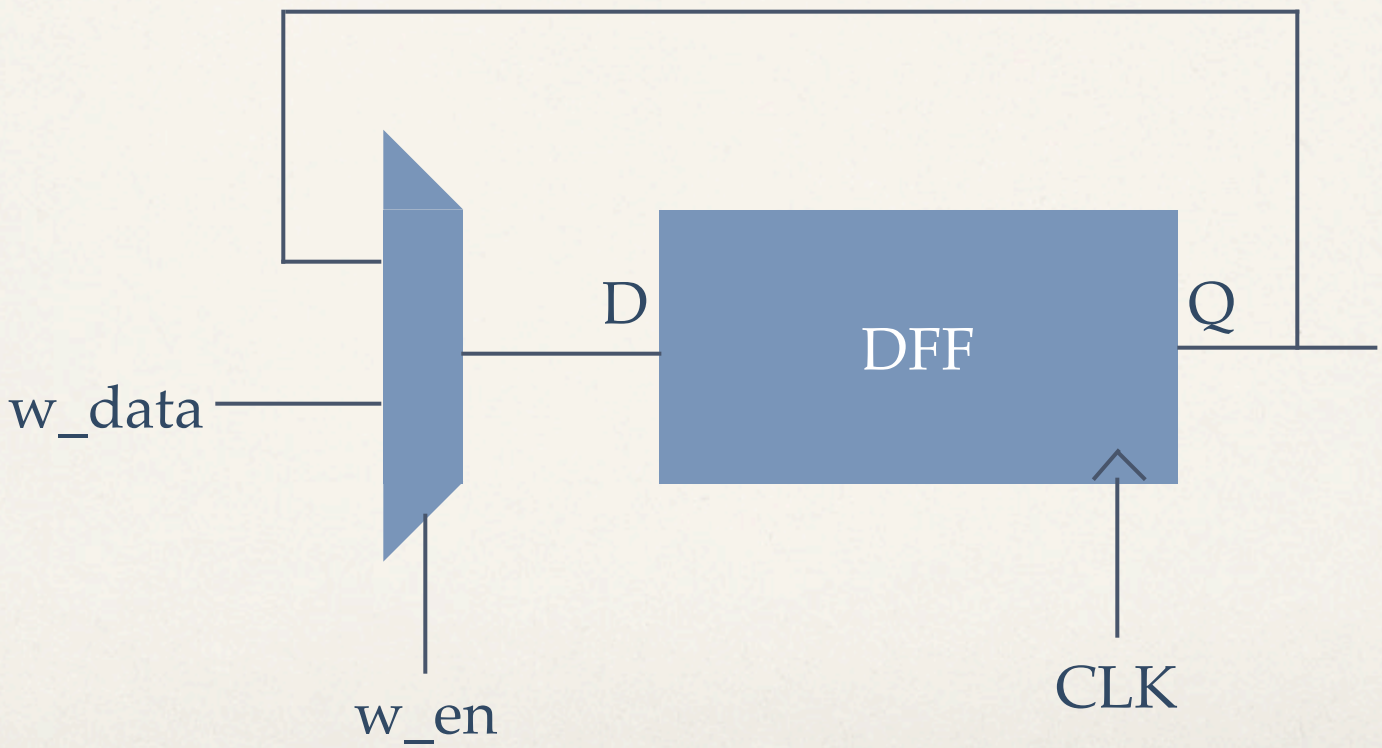
Any other questions?

- Any other questions on Lab 3?

Lab Tip: compile_ultra -gate_clock

```
1 //*****************************************************************************
2 // SMIPSv1 Register File
3 //-----------------------------------------------------------------------------
4 //
5
6 module smipsProcDpathRegfile
7 (
8   input         clk,
9   input  [ 4:0] raddr0,  // Read 0 address (combinational input)
10  output [31:0] rdata0,  // Read 0 data (combinational on raddr)
11  input  [ 4:0] raddr1,  // Read 1 address (combinational input)
12  output [31:0] rdata1,  // Read 1 data (combinational on raddr)
13  input         wen_p,   // Write enable (sample on rising clk edge)
14  input  [ 4:0] waddr_p, // Write address (sample on rising clk edge)
15  input  [31:0] wdata_p  // Write data (sample on rising clk edge)
16 );
17
18  // We use an array of 32 bit register for the regfile itself
19  reg [31:0] registers[31:0];
20
21  // Combinational read ports
22  assign rdata0 = ( raddr0 == 0 ) ? 32'b0 : registers[raddr0];
23  assign rdata1 = ( raddr1 == 0 ) ? 32'b0 : registers[raddr1];
24
25  // Write port is active only when wen is asserted
26  always @( posedge clk )
27  begin
28    if ( wen_p && (waddr_p != 5'b0) )
29      registers[waddr_p] <= wdata_p;
30  end
31
32 endmodule
```

Lab Tip: compile_ultra -gate_clock



Lab Tip: compile_ultra -gate_clock

Lab Tip: Result

Hierarchical cell	Global cell area: Absolute Total	Global cell area: Percent Total	Local cell area: Combi-national	Local cell area: Noncombi-national
smipsProc	128768.3828	100.0	11.0600	0.00
ctrl	3962.9443	3.1	1991.6417	0.00
ctrl/ir_FX	1239.5530	1.0	346.5309	893.02
ctrl/killF_mux	380.6149	0.3	380.6149	0.00
ctrl/statsEn_XM	43.3150	0.0	18.4320	24.88
ctrl/tohost_XM	307.8150	0.2	108.7510	199.06
dpath	124793.8984	96.9	3139.5098	0.00
dpath/alu	29100.1074	22.6	29100.1074	0.00
dpath/branch_cond_gen	852.2259	0.7	852.2259	0.00
dpath/op0_mux	1001.0535	0.8	1001.0535	0.00
dpath/op1_mux	1531.9567	1.2	1531.9567	0.00
dpath/pc_PF	1174.5323	0.9	378.2761	796.25
dpath/pc_inc4	740.0679	0.6	740.0679	0.00
dpath/pc_mux	1574.4377	1.2	1574.4377	0.00
dpath/pc_plus4_FX	796.2559	0.6	0.0000	796.25
dpath/rfile	82922.3828	64.4	58238.6289	24683.78
dpath/wb_mux	1959.9252	1.5	1959.9252	0.00
Total			101373.2188	27393.26

Hierarchical cell	Global cell area: Absolute Total	Global cell area: Percent Total	Local cell area: Combi-national	Local cell area: Noncombi-national	Local cell area: Black boxes
smipsProc	97727.8047	100.0	15.6680	0.0000	0.0000
ctrl	3597.1023	3.7	1709.8683	0.0000	0.0000
ctrl/ir_FX	1185.1509	1.2	330.8359	854.3149	0.0000
ctrl/killF_mux	350.2860	0.4	350.2860	0.0000	0.0000
ctrl/statsEn_XM	43.3150	0.0	18.4320	24.8830	0.0000
ctrl/tohost_XM	308.4770	0.3	74.3200	199.0640	0.0000
ctrl/tohost_XM/clk_gate_q_np_reg	35.0930	0.0	12.9750	22.1180	0.0000
dpath	94114.5938	96.3	2085.2571	0.0000	0.0000
dpath/alu	24047.6953	24.6	24047.6953	0.0000	0.0000
dpath/branch_cond_gen	790.5427	0.8	790.5427	0.0000	0.0000
dpath/op0_mux	886.4827	0.9	886.4827	0.0000	0.0000
dpath/op1_mux	1265.7739	1.3	1265.7739	0.0000	0.0000
dpath/pc_PF	1303.1644	1.3	506.9078	796.2559	0.0000
dpath/pc_inc4	737.4760	0.8	737.4760	0.0000	0.0000
dpath/pc_mux	1832.7324	1.9	1832.7324	0.0000	0.0000
dpath/pc_plus4_FX	796.2559	0.8	0.0000	796.2559	0.0000
dpath/rfile	58685.3711	60.0	32913.7148	24683.7891	0.0000
dpath/rfile/clk_gate_registers_reg_10_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_11_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_12_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_13_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_14_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_15_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_16_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_17_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_18_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_19_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_1_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_20_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_21_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_22_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_23_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_24_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_25_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_26_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_27_	35.0930	0.0	12.9750	22.1180	0.0000
dpath/rfile/clk_gate_registers_reg_28	35.0930	0.0	12.9750	22.1180	0.0000