Administrivia

- Midterm 1 is on **Monday 10:30 am in class**. One single-sided, letter-sized cheat sheet is allowed.
- PS3 will be released on next Wednesday.
- Lab2 due on **March 9th**.
Agenda

- PS2 Review
- Midterm 1 Review
  - Virtual memory
Microprogramming

- Decompose a complex instruction into multiple states
- Specify outputs for the current state and the next states
  - Optimize microinstructions to perform multiple actions if possible
  - Simplify control signals by using don’t care
Pipelining

- Iron Law: trade-offs between different designs
- Hazards - structural, data, and control hazards:
  - What implementations may cause the above hazards
  - How to solve them (hardware and software)
- CPI
  - How does CPI change with different bypath or datapath design
- Exceptions
  - Precise exception and how to implement it
Memory Hierarchy - Cache

- 3C’s
- Cache organization: associativity, replacement policy
- Cache optimizations (Lectures 6 & 7, discussion section 3)
- AMAT
Memory Hierarchy - Virtual Memory

- Paging vs Segmentation

<table>
<thead>
<tr>
<th></th>
<th>Page</th>
<th>Segment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Replace a block</td>
<td>Easy (fixed size)</td>
<td>Difficult (variable size, hard to find in main memory)</td>
</tr>
<tr>
<td>Inefficiency</td>
<td>Internal</td>
<td>External</td>
</tr>
<tr>
<td>Efficiency in disk</td>
<td>Yes (adjust page size to balance access</td>
<td>Not always (bad when the segment is small)</td>
</tr>
<tr>
<td>traffic</td>
<td>time and transfer time)</td>
<td></td>
</tr>
</tbody>
</table>
Memory Hierarchy - Virtual Memory

- Page Table Walk
  - Expensive
  - Software/Hardware
  - If page fault happens, OS handles that
- Are virtual and physical addresses necessarily the same width?
Memory Hierarchy - Virtual Memory

- TLB
  - Speed up address translation
  - Usually fully associative
  - Need to check protection bits
Memory Hierarchy - Virtual Memory

- Exercise 1
Memory Hierarchy - VIPT address aliasing

- **Aliasing**
  - \((\text{number of sets} \times \text{cache line size}) > \text{page size}\)
  - VA1 and VA2 are different at \([a]\) → point to different sets in cache
  - VA1 and VA2 point to the same PPN
  - Leads to multiple copies of same data in cache → coherence problem
Memory Hierarchy - VIPT address aliasing

- Exercise 2