Homework #3

Memory Hierarchy

This problem combines elements from chapter 7 and 8 problems. You have a 500 MHz processor with 2-levels of cache, 1 level of DRAM, and a DISK for virtual memory. Assume that it has a Harvard architecture (separate instruction and data cache at level 1). Assume that the memory system has the following parameters:

Component	Hit Time	Miss Rate	Block Size
First-Level Cache	1 cycle	4% Data 1% Instructions	64 bytes
Second-Level Cache	20 cycles + 1 cycle/64 bits	2%	128 bytes
DRAM	100ns+ 25ns/8 bytes	1$	16K bytes
TLB	1 cycle	0.1%	16K bytes

Finally, assume that the TLB has a fill penalty of 40 cycles.

Question 1: Assume that the DRAM miss rate refers to a page fault. The DISK parameters are: Drive rotates at 12000RPM, transfer rate 32 MB/second, 10ms average seek time. What is the "Miss Penalty" for filling a DRAM page? You can treat MB=10^6 bytes and KB=10^3 bytes.

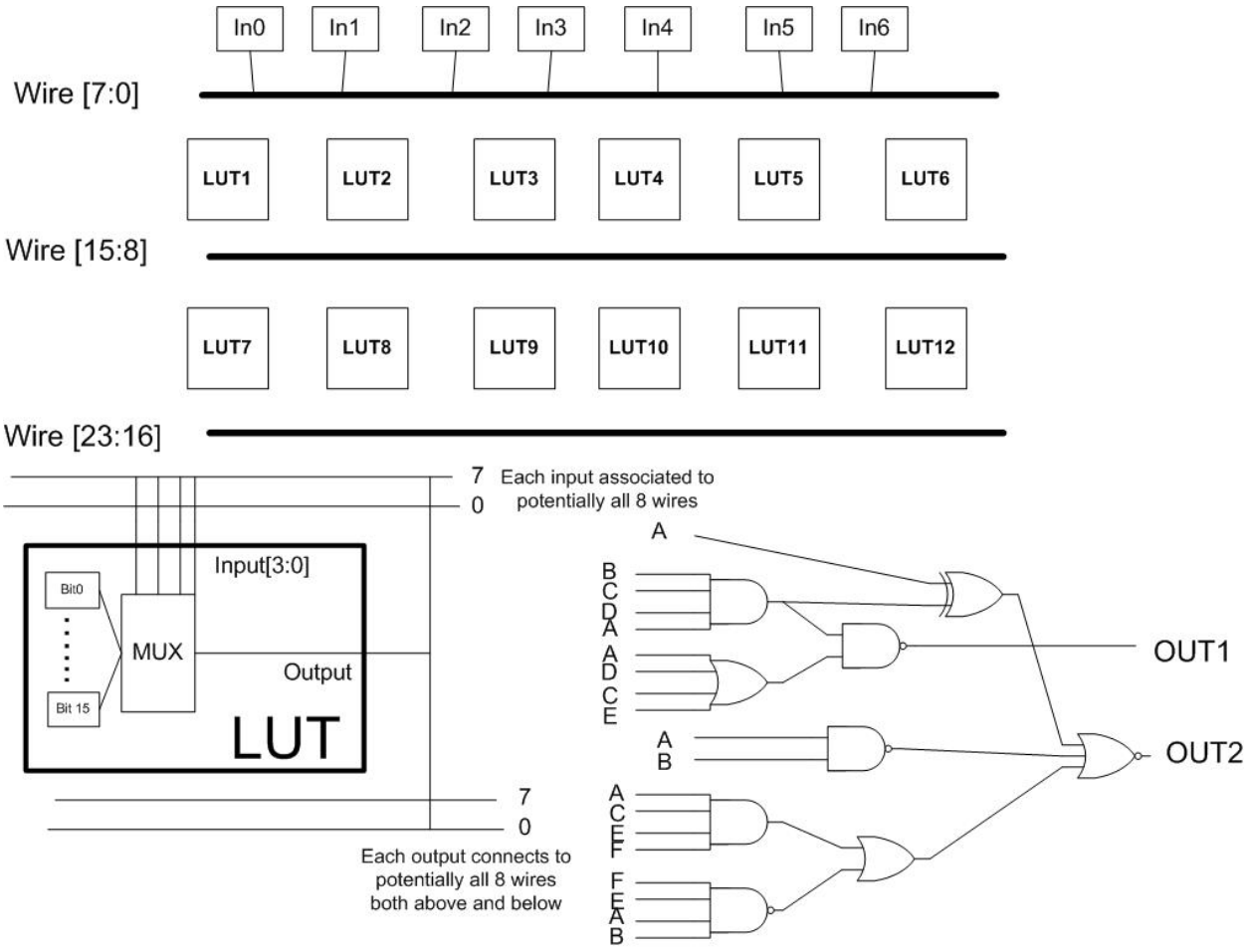
Miss penalty =

Question 2: Write an equation for $AMAT_{data}$ as seen by the processor. You do not have to generate an actual number. This equation should evaluate to a time in "ns", so make sure to check units.
Hint: using a set of equations with symbolic values is probably the simplest thing to do.

$AMAT_{data}$ =

FPGA Programming

For this question you will be implementing the digital circuit shown in the below figure on the FPGA based topology also shown in the figure. The topology includes 3 sets of 8 wires, 12 LUTs, and 7 input pads. The input pads are used to get input data to the circuit, the LUTs implement logic functions, and the wires are used to route input and output signals through the design.



1. Functional Programming

In order to begin, first define what bit values would be in the LUT registers (those feeding the LUT MUX) for the following gates which make up the circuit you will be implementing. Assume that for INPUT[3:0] = 0000 register 0 is selected and for INPUT[3:0] = 1111 register 15 is selected (i.e. the input value X corresponds to register X).

Fill out the following table with **"1" or "0"** for each entry as appropriate. It may be helpful to write out the input bit vector which will select each LUT register.

LUT Register	AND4	OR4	NAND4	NAND2	OR2	XOR2	NOR3
0							
1							
2							
3							
8							
12							
13							
14							
15							

Table 1: LUT Programming

*For the gates of less then 4 inputs, assume that for 2 inputs you use INPUT[3:2] and for 3 inputs you use INPUT[3:1]. You are looking at the "Most Significant Bits". This means that the other input(s) in these cases are DON'T CARES.

2. Placement and Routing

Now you will determine which LUTs to use to implement which function and how to connect them to realize the functionality specified in the circuit diagram. **The next items (a, b) you should consider simultaneously since they potentially effect each other**. If it is easier to understand feel free to **label the circuit diagram** (both the wires for which "real wires" they will connect to and the gates as to which LUT they correspond to) and then transfer your answers to the blanks provided (strongly recommended). **Label what is given first then design around it.**

a. What input signal should be assigned to which input pad (A, B, C, D, E, F)? Leave blank if input pad not used. Each input pad can connect to any of the 8 wires on the set of wires "Wire[7:0]". Which wire(s) should each input be connected to (i.e Wire0)? Naturally leave blank if the pad is not used. Part of the table is completed for you. **(X pts)**

Pad	Input Signal	Wire Assignment
In0		
In1	A	Wire 0
In2		
In3	B	
In4	D	Wire 4
In5		Wire 1
In6		

Table 2: Input Assignment

b. For each LUT specify which functionality should be placed there (NAND4, OR4, AND4, NAND2, XOR2, OR2, NOR3). Leave blank if that LUT will not be assigned. **(X pts)**
   i. Each input of a LUT can potentially connect to any of the 8 wires on the collection "above it". Which wire(s) should each LUT input connect to? In the event that the input is not needed, just put dashes "-" there. In the event that you do not need the LUT also just leave the entry blank. **(X pts)**
   ii. The output of each LUT can potentially connect to any of the eight wires **"above" it or "below" it.** Which wire(s) should each LUT output connect to? In the event that the output is not needed, just leave it blank. In the event that you do not need the LUT also just leave the entry blank. **(X pts)**

LUT	Function	Input0	Input1	Input2	Input3	Output
1		0	4	2	1	
2	AND4					11
3						7
4						
5		--------	-------			15
6					3	
7						
8						
9	OR2					
10		-------	--------			
11		-------				17
12						

Table 3: LUT Assignment and Routing

c. What wire will the final outputs of the circuit be on?
OUT1 ____ OUT2 ____

3. Design Decisions and Economic Impact

The next set of questions is regarding design issues and the economic effect of those design decisions as they relate to FGPAs. Please circle "True" or "False". If false make a brief statement why this is the case.

a. True or False – All FPGAs are required to have the routing structure in the diagram provided.
If False: _____

b. True or False – Placement and routing software is independent of the specific FPGA.
If False: _____

c. True or False – Since FPGAs typically cannot run at a high clock rate they will not perform (as measured by execution time) as well as a general purpose microprocessor (like Pentium) for ANY application.
If False: _____

d. True or False – FPGAs are typically more expensive to the customer as compared to ASICs.
If False: _____

e. True or False – FPGA's regular architecture (i.e. blocks of CLBs and routing resources) contribute to its lower than ASIC NRE costs.
If False: _____

f. True or False – The expression "AB + CD" has to be implemented as a set of AND gates and a single OR gate on the FGPA design provided in the previous section.
If False: _____

g. True or False – The FPGA you use in the lab is the Calinx FPGA.
If False: _____

Bonus Question: What is the theoretical maximum circuit depth (i.e. gates in a row) that this FPGA topology could support?