Problem set 4 solutions

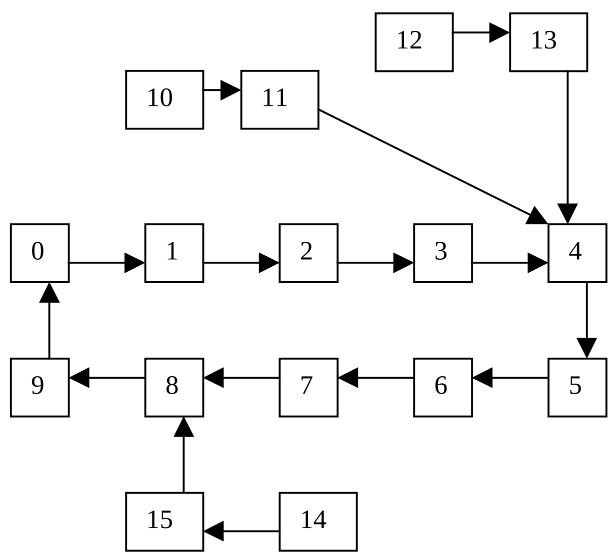
7.10 We're designing a counter that counts from 0 to 9 and returns to 0, so we'll implement with 4 bits, and encode the states in binary. Because we only need 10 states, we'll have six rows of "don't care", which will make the implementation logic easier. Of course, depending on how the "don't care's" end up being implemented, we might

	Q3	Q2	Q1	Q0	Q3+	Q2+	Q1+	Q0+	T3	T2	T1	T0	S3	R3	S2	R2	S1	R1	S0	R0	J3	K3	J2	K2	J1	K1	J0	K0
0	0	0	0	0	0	0	0	1	0	0	0	1	0	x	0	x	0	x	1	0	0	x	0	x	0	x	1	x
1	0	0	0	1	0	0	1	0	0	0	1	1	0	x	0	x	1	0	0	1	0	x	0	x	1	x	x	1
2	0	0	1	0	0	0	1	1	0	0	0	1	0	x	0	x	x	0	1	0	0	x	0	x	x	0	1	x
3	0	0	1	1	0	1	0	0	0	1	1	1	0	x	1	0	0	1	0	1	0	x	1	x	x	1	x	1
4	0	1	0	0	0	1	0	1	0	0	0	1	0	x	x	0	0	x	1	0	0	x	x	0	0	x	1	x
5	0	1	0	1	0	1	1	0	0	0	1	1	0	x	x	0	1	0	0	1	0	x	x	0	1	x	x	1
6	0	1	1	0	0	1	1	1	0	0	0	1	0	x	x	0	x	0	1	0	0	x	x	0	x	0	1	x
7	0	1	1	1	1	0	0	0	1	1	1	1	1	0	0	1	0	1	0	1	1	x	x	1	x	1	x	1
8	1	0	0	0	1	0	0	1	0	0	0	1	x	0	0	x	0	x	1	0	x	0	0	x	0	x	1	x
9	1	0	0	1	0	0	0	0	1	0	0	1	0	1	0	x	0	x	0	1	x	1	0	x	0	x	x	1
10	1	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
11	1	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
12	1	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
13	1	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
14	1	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
15	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

7.10 part b continued) To implement the counter in T, SR, and JK flip-flops, we first need to write down the excitation for those flip-flops based on the current state and next state (above).
Notice that the columns for the SR and JK flip flops are identical, except that where ever the SR pair was a 01 the JK pair is an x1, and whenever the SR was a 10, the JK is a 1x. K-maps and functions are below and on the following page.

Part c) For the D-FF implementation, based on what I circled in the K-maps, I fill in the ‘x’s as 1s or 0s, and figure out where my “don’t care” states ended up. As it turns out, they all eventually go to the main sequence, so this is a self starting counter.

	Q3	Q2	Q1	Q0	Q3+	Q2+	Q1+	Q0+	
0	0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	0	1	0	2
2	0	0	1	0	0	0	1	1	3
3	0	0	1	1	0	1	0	0	4
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	1	0	6
6	0	1	1	0	0	1	1	1	7
7	0	1	1	1	1	0	0	0	8
8	1	0	0	0	1	0	0	1	9
9	1	0	0	1	0	0	0	0	0
10	1	0	1	0	1	0	1	1	11
11	1	0	1	1	0	1	0	0	4
12	1	1	0	0	1	1	0	1	13
13	1	1	0	1	0	1	0	0	4
14	1	1	1	0	1	1	1	1	15
15	1	1	1	1	1	0	0	0	8



T3 (Q3, Q0, Q1, Q2)

0	0	x	0
0	0	x	1
0	1	x	x
0	0	x	x

T2 (Q3, Q0, Q1, Q2)

0	0	x	0
0	0	x	0
1	1	x	x
0	0	x	x

T1 (Q3, Q0, Q1, Q2)

0	0	x	0
1	1	x	0
1	1	x	x
0	0	x	x

T0 (Q3, Q0, Q1, Q2)

1	1	x	1
1	1	x	1
1	1	x	x
1	1	x	x

T3=Q3Q0+Q2Q1Q0 T2=Q1Q0 T1=\Q3Q0 T0=1

T3

			Q3		
	0	0	x	0	
	0	0	x	1	Q0
Q1	0	1	x	x	
	0	0	x	x	
		Q2			

T2

			Q3		
	0	0	x	0	
	0	0	x	0	Q0
Q1	1	1	x	x	
	0	0	x	x	
		Q2			

T1

			Q3		
	0	0	x	0	
	1	1	x	0	Q0
Q1	1	1	x	x	
	0	0	x	x	
		Q2			

			Q3	
	1	1	x	1
	1	1	x	1
Q1	1	1	x	x
	1	1	x	x
		Q2		