Quiz 2
Room 10 Evans, Tuesday 3/31
(Open Katz, Calculators OK, 1hr 20min)

Include all final answers in locations indicated on these pages. Use reverse side of sheets for all working. If necessary, attach additional sheets by staple at the end. BE SURE TO WRITE YOUR NAME ON EVERY SHEET.

(1) (a) The binary string “10110101” is the 8-bit two’s complement representation of a fixed point number. What is its decimal value?

1(a) (5pts)

\[
10110101 = \quad \text{___10}
\]

(b) Design a circuit to compute the two’s complement of a 3-bit binary number. The inputs are b₀, b₁ and b₂, where b₂ is the most significant digit and the outputs are c₀, c₁ and c₂ where c₂ is the most significant digit.

(i) Show a truth table for the circuit.
(ii) Draw Karnaugh maps for each output and use them to simplify the functions.
(iii) Draw a schematic diagram using the minimum number of NAND gates and inverters only.

1(b) (15pts)

(i) Truth table:

1(b) (ii) Karnaugh Maps:
(iii) Schematic diagram:
You are to design a “Manhattan Compass” which is an automobile accessory which has four display lights labelled North, South, East, and (yes, you guessed it...) West. One of the lights is always lit and indicates which direction the car is facing. There are two sensors on the steering wheel, labelled Right and Left. The wires connected to each of the right and left sensors has the value 1 when the position of the steering wheel is to the right or left of center respectively and a value of 0 otherwise. In addition, there is a button labelled INIT which, when pushed, tells the system that the car is stationary, the steering wheel is centered (neither right nor left) and the car is facing north. In Manhattan, all turns are exactly 90 degrees once initiated (U turns are not permitted). Your design is to be a clocked synchronous circuit of the Moore form. Assume the clock signal CLK is derived from the left and right signals.

(a) Provide a state transition graph for a Moore implementation of the compass. Use the minimum number of states.

(b) Provide a state table for the compass.

(c) Derive the flip-flop input equations and compass output equations for an implementation which uses clocked D flip-flops. Assume the INIT signal is used to reset the flip flops. Draw a schematic diagram for your circuit, including the D flip-flops and a minimum number of logic gates (no multiplexors!). Show all Karnaugh maps used.
2(c)  (i) (2pts) Karnaugh Maps:

(ii) (6pts) Flip-flop Input Equations & clock generation:

_____________________________________________

_____________________________________________

CLK = _____________

(iii) (4pts) Output Equations:

N = ________________  E = ________________

S = ________________  W = ________________

(iv) (7pts) Schematic Diagram:
(3) Consider the state table for a Mealy machine shown below:

<table>
<thead>
<tr>
<th></th>
<th>next state</th>
<th>output Z</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>x=0</td>
<td>x=1</td>
</tr>
<tr>
<td>$S_0$</td>
<td>$S_1$</td>
<td>$S_2$</td>
</tr>
<tr>
<td>$S_1$</td>
<td>$S_3$</td>
<td>$S_2$</td>
</tr>
<tr>
<td>$S_2$</td>
<td>$S_1$</td>
<td>$S_4$</td>
</tr>
<tr>
<td>$S_3$</td>
<td>$S_5$</td>
<td>$S_2$</td>
</tr>
<tr>
<td>$S_4$</td>
<td>$S_1$</td>
<td>$S_6$</td>
</tr>
<tr>
<td>$S_5$</td>
<td>$S_5$</td>
<td>$S_2$</td>
</tr>
<tr>
<td>$S_6$</td>
<td>$S_1$</td>
<td>$S_6$</td>
</tr>
</tbody>
</table>

(a) Draw a **state transition graph** for the machine showing all input/output transitions and symbolic states.

(b) Use the **guidelines presented in class for state assignment** to select an optimal state assignment (for minimum logic). **Show all constraints**, your **final state assignment**, and indicate **which constraints are not satisfied by the assignment**.

(c) If a **ROM where used to implement the next-state and output logic** for a **D-flip-flop-based implementation** of your machine, how big would it have to be?

3(a) (4 pts) State Transition Graph:
3(b) (i) (6 pts) Constraints:

Guideline 1: _________________________________
Guideline 2: _________________________________
Guideline 3: _________________________________

(ii) (3 pts) Karnaugh Map for Assignment:

```
   0  00  01  11  10
  0  0  2  6  4
  1  1  3  7  5
```

(iii) (3 pts) Final State Assignment:

S0 = _____  S1 = _____  S2 = _____
S3 = _____  S4 = _____  S5 = _____  S6 = _____

(iv) (3 pts) Constraints not satisfied:

____________________________________________________________________
____________________________________________________________________

3(c) (6pts) ROM size:

Number of address lines: ______
Number of data bits at each address: ______
Total number of ROM bits: ______