Banks 14, 16, 18, 21
DDR2, PS2, GPIO
Unused banks on the LX50T and SX50T

Banks 15, 17
VGA, IIC, PHY
SRAM, FLASH, GPIO

Title: Banks 11, 12, 13
VGA, IIC, PHY, SRAM, GPIO

ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1200415
0391241

Date: 1-22-2008_14:51
Rev: A
Sheet: 5 of 27
Drawn By: A
Diff Clocks: SMAs, Generation, MUX and Buffer

System Clock Generation

User Clock

Clocking - Differential Clock, System Clock & User Clock

Title: Differential Clock, System Clock, User Clock

Sheet Size: B
Rev: D2
Sheet 9 of 27
Drawn By: 99

Diff Clocks: SMAs, Generation, MUX and Buffer
XGI Expansion Interface

Matched Length Traces

VCC3V3

Rev: B

VCCO_EXP

IIC_SCL_MAIN

GPIO_LED_E

GPIO_LED_S

EXPANSION_TDO

FPGA_EXP_TMS

FPGA_EXP_TCK

NC

PC4_HALT_B

CPU_TMS

CPU_TCK

FPGA_CS0_B

CPU_TRST

MICTOR_18

TRC_TS2E

TRC_TS4

TRC_TS5

MICTOR 38

1-22-2008_14:51

MICTOR 38

XGI - Expansion Connectors

Mark Pin 1

Pin 14 must be removed.

XGI - Expansion Headers

ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1200415

SCHEM, ROHS COMPLIANT

Title: XGI - Expansion Headers

Drawn By: A

Rev: A

Sheet 11 of 27

Date: 1-22-2008

Sheet Size: B

Ver: 02

MICTOR 38

VCC5

IIC_SDA_EXP

GPIO_LED_N

GPIO_SWM

GPIO_LED_W

GPIO_LED_N

EXPANSION_TDO

FPGA_EXP_TMS

FPGA_EXP_TCK

NC

PC4_HALT_B

CPU_TMS

CPU_TCK

FPGA_CS0_B

CPU_TRST

MICTOR_18

TRC_TS2E

TRC_TS4

TRC_TS5

MICTOR 38

1-22-2008_14:51

MICTOR 38

XGI - Expansion Connectors

Mark Pin 1

Pin 14 must be removed.
The PHY MDIP Pins below are Media Dependent Interface Pins (MDIP), and are all bidirectional pins.

- J22, J23 pins 1-2: OMNI/MEI to Cu
- J22, J23 pins 2-3: OMNI to Cu, no silk
- J22 pins 1-2, J24 OM: OMNI, modified MEI in Cu

Pin to Constant Mapping

<table>
<thead>
<tr>
<th>Pin</th>
<th>Bit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC2V5</td>
<td>011</td>
<td>110</td>
</tr>
<tr>
<td>LED_LINK10</td>
<td>101</td>
<td></td>
</tr>
<tr>
<td>LED_LINK100</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>LED_LINK1000</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>LED_DUPLEX</td>
<td>101</td>
<td></td>
</tr>
<tr>
<td>LED_RX</td>
<td>101</td>
<td></td>
</tr>
<tr>
<td>LED_TX</td>
<td>001</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>000</td>
<td></td>
</tr>
</tbody>
</table>

Title: 10/100/1000 PHY
Author: ROHS COMPLIANT
ML605/7 VIVADO'S EVOLUTION PLATFORM, 1200415
10/100/1000 PHY
Sheet 1 of 27
Drawn By: A
IIC Address = 0x4C

VGA In Codec

VGA In Codec
The burst order mode of the SRAM is set to "Linear" by default.
MGT PLL Regulator

Voltage Output Settings

AVCC_PLL = 1.2V @ 3A
R176 = 2.43K 1%
R177 = 4.99K 1%

FXT Only (ML507)
AVCC_PLL = 1.0V @ 3A
R176 = 1.13K 1%
R177 = 4.53K 1%

MGT AVCC Regulator

MGT VTT Regulator

MGT RXC Regulator

MGT Power Supplies
5V and 3.3V Power Supplies

3.3v to 2.5V (VCC AUX) Regulator

5V to 0.9V (DDR VTT VREF) Regulator

3.3v to 2.5V Regulator

5V to 0.9V (DDR2 VTT DDR) Regulator

5V and 3.3V Power Supplies