

EECS150 - Digital Design

Lecture 8 - Multipliers (part 1):

Design Example

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Multiplication

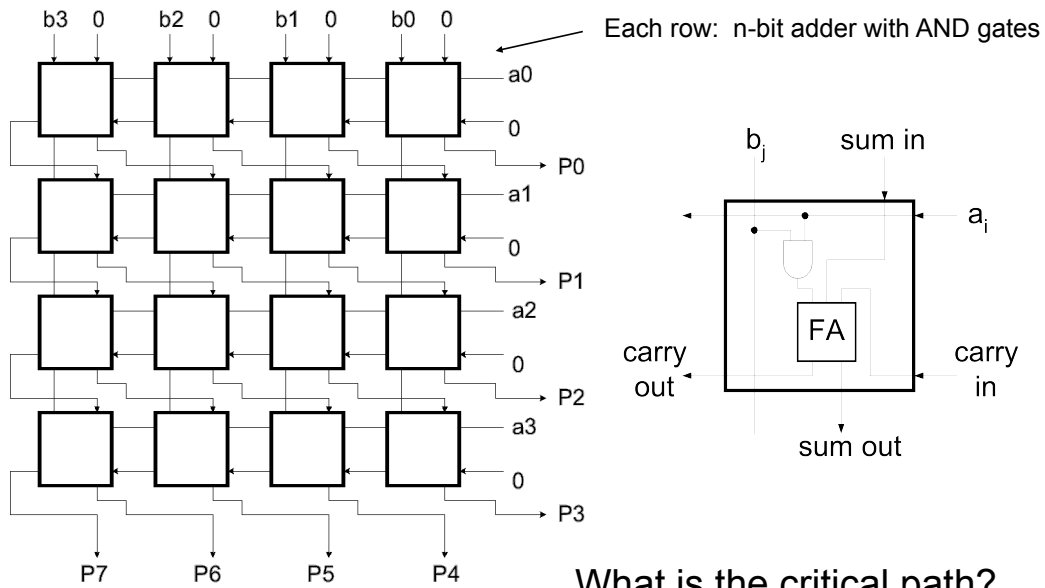
a_3	a_2	a_1	a_0	\leftarrow <i>Multiplicand</i>	
b_3	b_2	b_1	b_0	\leftarrow <i>Multiplier</i>	
	X	a_3b_0	a_2b_0	a_1b_0	a_0b_0
		a_3b_1	a_2b_1	a_1b_1	a_0b_1
		a_3b_2	a_2b_2	a_1b_2	a_0b_2
a_3b_3	a_2b_3	a_1b_3	a_0b_3		
		\dots	$a_1b_0 + a_0b_1$	a_0b_0	\leftarrow <i>Product</i>

$\left. \begin{array}{l} a_0b_0 \\ a_0b_1 \\ a_0b_2 \\ a_0b_3 \end{array} \right\} \text{Partial products}$

*Many different circuits exist for multiplication.
Each one has a different balance between
speed (performance) and amount of logic (cost).*

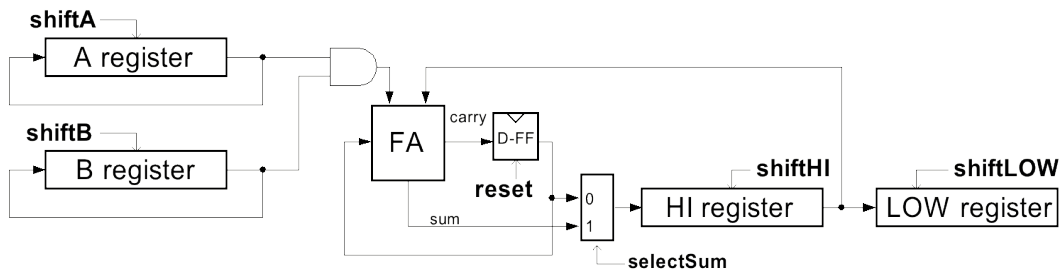
Array Multiplier

Single cycle multiply: Generates all n partial products simultaneously.



Bit-Serial Multiplier

- Example, Bit-serial multiplier (n^2 cycles, one bit of result per n cycles):



- Control Algorithm:


```

repeat n cycles { // outer (i) loop
  repeat n cycles{ // inner (j) loop
    shiftA, selectSum, shiftHI
  }
  shiftB, shiftHI, shiftLOW, reset
}
      
```

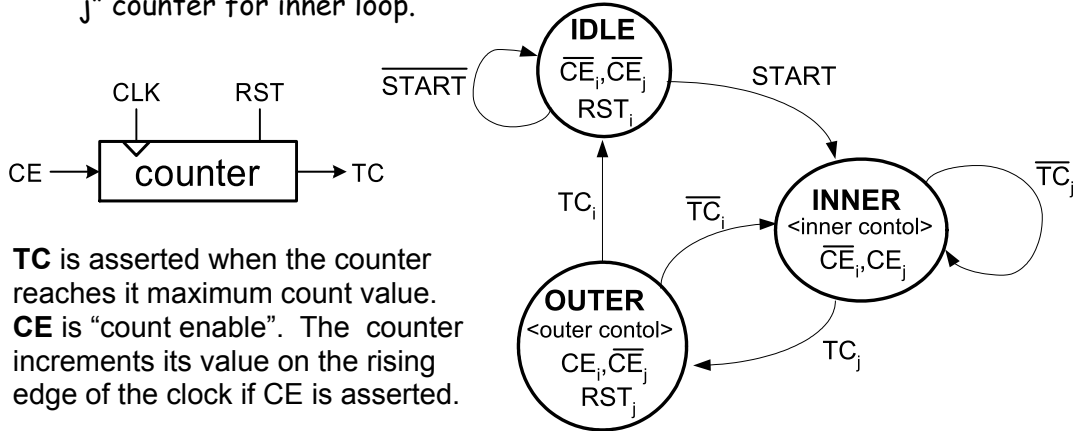
Note: The occurrence of a control signal x means $x=1$. The absence of x means $x=0$.

Controller using Counters

- **State Transition Diagram:**

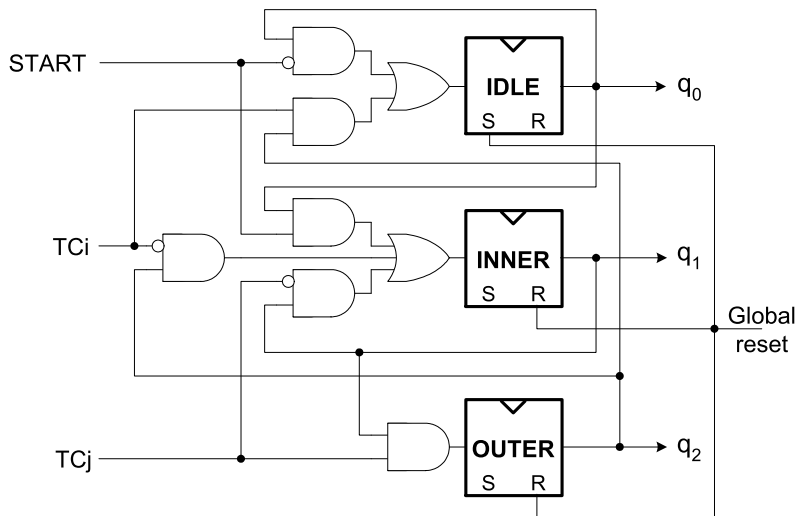
- Assume presence of two binary counters. An "i" counter for the outer loop and "j" counter for inner loop.

```
repeat n cycles { // outer (i) loop
  repeat n cycles{ // inner (j) loop
    shiftA, selectSum, shiftHI
  }
  shiftB, shiftHI, shiftLOW, reset
}_
```



Controller using Counters

- **Controller circuit implementation:**



- **Outputs:**

$$\begin{aligned} CE_i &= q_2 \\ CE_j &= q_1 \\ RST_i &= q_0 \\ RST_j &= q_2 \end{aligned}$$

$$\begin{aligned} \text{shiftA} &= q_1 \\ \text{shiftB} &= q_2 \\ \text{shiftLOW} &= q_2 \\ \text{shiftHI} &= q_1 + q_2 \\ \text{reset} &= q_2 \\ \text{selectSUM} &= q_1 \end{aligned}$$