University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2012

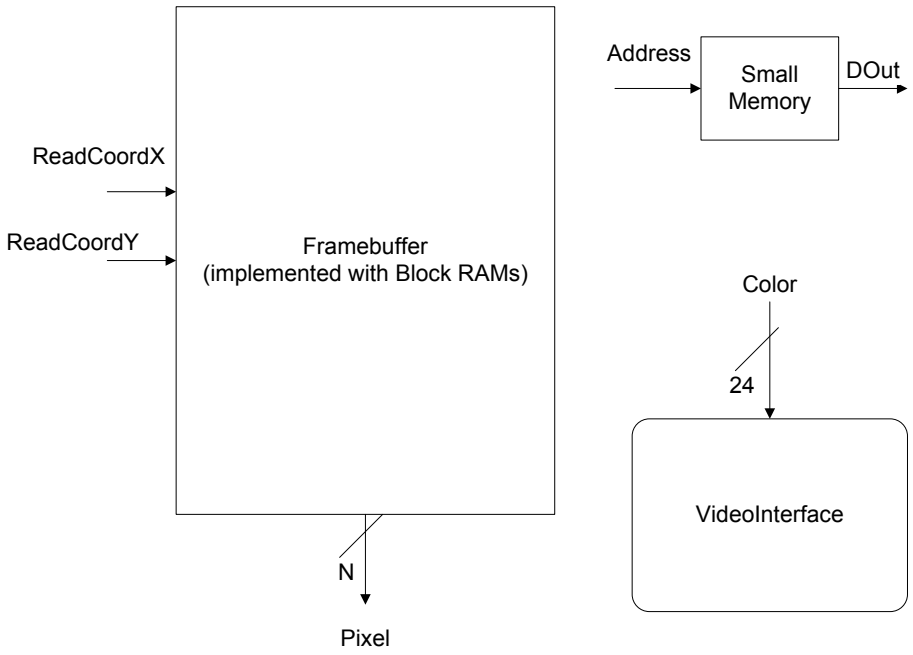
Homework Assignment 8: Video, Synchronizer
Due March 15^{th}, 2pm

1. Suppose we implement our 1024x768 pixel framebuffer using the Block RAM resources on our XC5VLX110T FPGA. You can look in Virtex-5 Family Overview on the Documents page of the website for the resources available on different Virtex-5 FPGA models. Suppose a quarter of the Block RAMs on the fpga are being used for our instruction and data memories already, leaving three quarters for the framebuffer

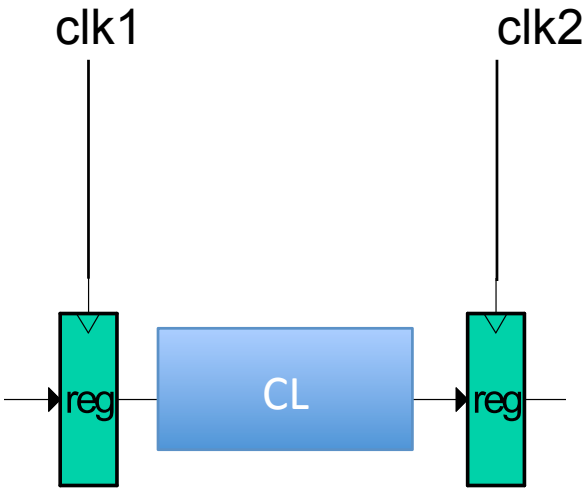
   (a) How many bits are available for each pixel?

   (b) How many distinct colors can be represented? (Let this number be hereafter called N)

   (c) Recall that our video interface supports 24-bit color. How can you use a relatively small memory to allow any N of the 2^{24} displayable colors to be used at a given time? Draw a high level block diagram of the framebuffer, video interface, and the extra memory block implementing this functionality. Specify the dimensions of the small memory.



2. In the circuit below, clk1 is running at 100MHz, clk2 is running at 75MHz, both registers have $T_{setup} = T_{hold} = 1ns$, $T_{c2q} = 1.5ns$. Also, it is known the CL block has a delay of $5ns$. Assume at time=0, both clk1 and clk2 are having a rising edge, is there a possibility of flip-flop failure due to metastability? If so, when might that occur? If not, explain why.


clk1
clk2
reg
CL
reg