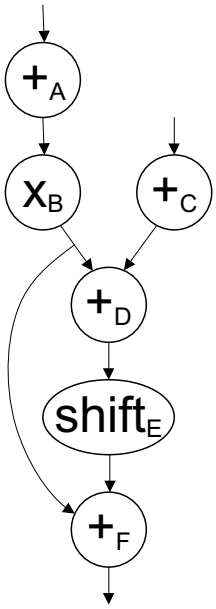
**University of California at Berkeley**
**College of Engineering**
**Department of Electrical Engineering and Computer Science**

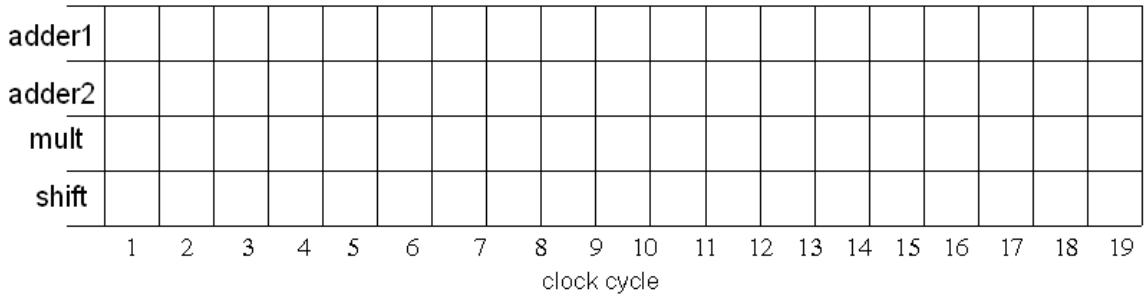
EECS150, Spring 2012

**Homework Assignment 11: High-level Design**
**Due April $26^{th}$, 2pm**

1. Imagine a datapath that has four computation units; two adders, a multiplier, and a shifter. Each unit requires an entire clock cycle (minus flip-flop overheads) to complete its operation and is followed by a register to hold its output. The graph below represents an iterative operation to be completed on the datapath. Each node is labeled with the name of the computation unit it requires plus a unique letter identifying the node. Note that there is no feedback (or loop carry dependence) in this computation.




Use modulo scheduling to show how to complete four iterations of the loop in the minimum number of cycles. Show your work. Then, in the chart shown below the unique integer node numbers from the graph. Use subscripts (1, 2, 3, and 4) to indicate the iteration number. For instance, C2 indicates node C of iteration 2.




2. Consider the design of a special processor connected to a dual-ported memory, shown below. In the memory, an array of 8-bit integers is stored, starting at address 0. When started, the processor begins at location 0 and moves through memory forming the sum of all the integers up to that point, storing the sum in each memory location as it goes. The process continues for the entire array. An input signal call **START** is used to start the process, and an input called **ENDADDR** is used to specify the address of the final element in the array.

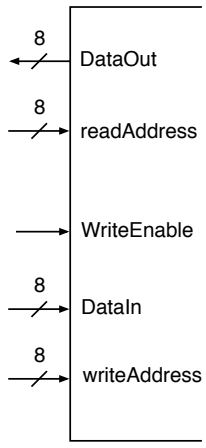
   Write the register transfer language description of the processor operation and draw the design of the processor datapath.

   • Use only the following circuit elements:

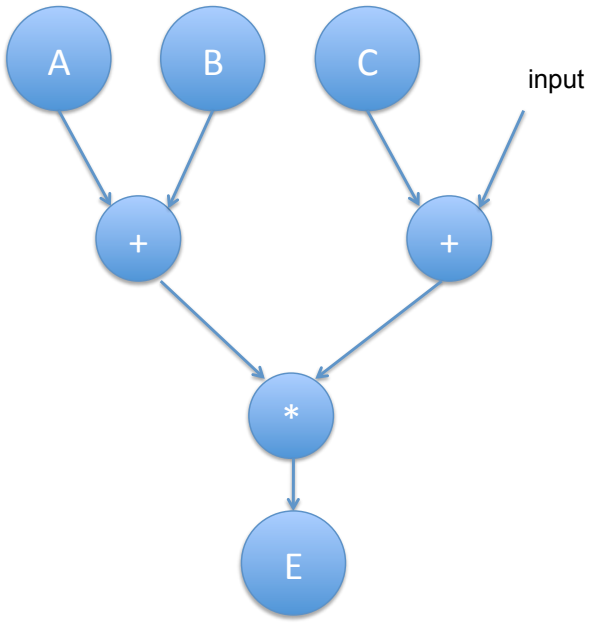
   (a) binary adder(s) of any width
   (b) register(s) with reset and load-enable,
   (c) equal-comparator(s), and the memory show below. The memory has asynchronous read and synchronous write operations.

   • In your design, minimize the processor cycle time and the number of cycles in the innerloop.

   • Remember to use a comma, ",", to separate RTL operations that occur on the same clock cycle, and a ";" to seperate operations on different cycles.



3. The graph below shows the computation that happens in one iteration. The circles A, B and C represent LOADs from the memory, the circle E represents a STORE operation to the memory. The other circles are labelled with the computation each represents. You may assume you have two adders, a true dual port memory (each port can support an independent read/write), and a non-pipelined multiplier, also the multiplication would take two cycles to complete while the addition and memory operations only take one cycle.




   (a) If you have no information about the addresses that each of the LOADs and STOREs use, how would you schedule the operations? Show your schedule for four iterations.

   (b) After alias analysis is done on the application, it can be safely assumed that the addresses E stores would never be loaded by A, B or C. How would you schedule the operations now? Again, show four iterations.

4. Explain how the C-slow technique increases the throughput. It is observed that when this technique is applied to FPGA implementations, the addition of the first couple of threads would increase the throughput, but the performance starts degrading as more threads are added. What do you think is the main reason for this? Do you think this problem would be more or less serious if ASIC is used?

5. How do you design a SEC, DED code for 64 bit data? State the positions of the parity bits, and which bits of the codeword each parity bit protects. (Since there are many bits, you might want to express the bit number in terms of variables, and then give a range of the variable.)

6. A student (A) decides to duplicate his datapath in an accelerator such that the compute throughput can be increased by 2X (you can assume the application contains enough parallelism for this to happen) when he runs the accelerator at the same clock frequency.

(a) The other student tries to match this performance gain by increasing the voltage of his circuit (assume the max frequency a CMOS circuit is positively related to the voltage at which it runs). In terms of dynamic power consumption, do you think his solution is better or worse than that of student A ? Why?

(b) With the duplicated datapath, student A can afford to reduce the clock frequency by half yet still achieve the throughput of the original accelerator. If he does not lower the voltage of the circuit, how does this reduction of clock frequency effect the overall power of the circuit? How does it effect the overall energy consumption for running the application? Explain your reasoning. (Note: the baseline used in this question is the accelerator with a duplicated datapath.)