University of California at Berkeley
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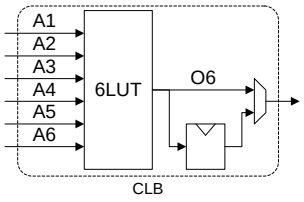
EECS150, Spring 2010

Quiz 9: April 2^{nd}
10 Minutes

Consider a system with generic FPGA architecture with 6-input LUTs and flip-flops, as shown below.



The timing characteristics of this system are detailed below:

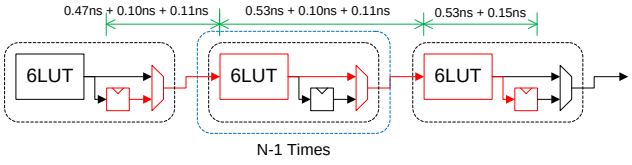
- The shortest delay through the global routing fabric is 0.11 ns.
- The shortest delay through the 6LUT is 0.15 ns.
- The longest delay through the 6LUT is 0.53 ns.
- The delay through the MUX is 0.10 ns.
- The register Clock to Q delay is 0.47 ns.
- The flip-flop setup time is 0.15 ns.
- The flip-flop hold time is 0.24 ns.

Use this data to answer the following questions:

1. When building a 10 MHz processor, what is the largest number of consecutive LUTs allowed in one pipeline stage?

   The clock period in this system is 100ns.

   Any path from flip flop to flip flop will look like this:



We simply have to solve for N in $100ns \geq (0.47ns + 0.10ns) + (N-1)(0.11ns + 0.53ns + 0.10ns) + (0.11ns + 0.53ns + 0.15ns)$. The answer is 134 consecutive LUTs.

2. When building a shift register (using flip-flops), how much clock skew can the system tolerate without violating hold time?

The path follows the same pattern as in the solution above, but we are now fixing N at 1, and solving for the largest subtractive term (clock skew). $0.24s \leq (0.47ns + 0.10ns + 0.11ns + 0.15ns + 0.15ns) - (skew)$. The answer is 0.74ns.