University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Quiz 12: April 23^{rd}
15 minutes

1. How many 1-bit adder cells are needed to implement an unsigned 16x16-bit multiplier using the following schemes:

   (a) A combinational array multiplier _____ full adder cells

   (b) A bit-serial multiplier _____ full adder cells

2. Now one of the adder inputs is hard-wired to a constant 16'd37 (16'h25).

   (a) How many bits of addition can be saved in comparison to the array multiplier by taking advantage of the constant?
   . _____ full adder cells

   (b) Draw the circuit for an unsigned 16-bit multiply-by-37 circuit below. Ignore overflow conditions. You may use an N-bit adder block (assume a ripple adder implementation) in your answer.