Lab Logistics & FPGA Editor

UCB EECS150 Spring 2010

Lab Lecture #1

Agenda

- Lab Logistics
  - Lab lecture
  - Labs in general
  - Lab policies
- Questions?
- Class Hardware
- FPGA Editor (CAD Tool)
- Lab #1
  - Contents
  - Pre-lab
- Questions?

Lab Lecture (1)

- Components
  (1) Weekly quiz
  (2) 'Lecturette' from a T.A.
- Motivation
  - Learn about the next week's lab
  - Have a chance to ask questions
- To get the most out of this…
  - Do the homework
  - Read the lab [before lab lecture]

Lab Lecture (2)

- Resources
  - In-lab HD audio & video, mic, projectors, CCTV
  - T.A. {him/her} self
    - Again, ask questions!
    - Sit where you can actually see the T.A.
  - Lab materials
    - Slides will be posted ahead of time
    - Lab *.zip file ~ contains:
      - Verilog, support files
      - Lab documents (+ what is required at check-off)

Labs (1)

- Each lab consists of…
  - (1) Lab lecture — Friday (end of week 0)
  - (2) Lab period — Tues/Wed/Thurs* (week 1)
  - (3) Check-off — Tues/Wed/Thurs* (week 2)

  * During your assigned lab period
- Check-off procedure
  - Lab T.A. will walk around the room in desk order
  - You are required to…
    - (1) Show your T.A. the completed check-off sheet
    - (2) Present all required demos

Labs (2)

- Partner policy
  - The labs are about learning the tools
    … which everyone must do to pass this class
  →Labs are done alone
- Projects are done in groups of two
  - Odd enrollment handled on a case-by-case basis
  - Project Check-off
    - Partners should be able to *attend* the same lab
    - But do not have to be *enrolled* in the same lab
    - More details on this closer to the project

Lab Policies (1)

We all share the same lab.
Treat it with care!

- General Policies
  - At the lab stations
    - No food, drink, bikes, etc
  - At the white tables
    - Feel free to eat/drink
    - In all cases, clean up after yourself
    - This area will be used for discussion sections/office hours
  - Lab-wide
    - **NO** alcohol (all Campus policies apply)
    - **Clean up your trash**

Lab Policies (2)

- Lab Usage
  - Section A/C*
    - EECS 150 has priority on space/computers
    - Feel free to work on other course work
  - Section B*
    - Being used for another class

*: When in doubt: if the station doesn't have an XUPv5, you won't be able to use it!

  - T.A. Station: off-limits
  - Learn the lab orientation

Lab Policies (3)

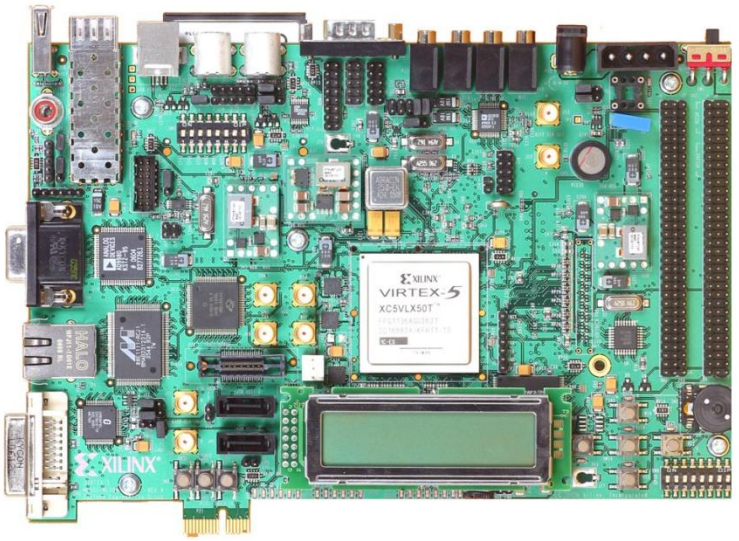
- Lab Access
  - Doors
    - Everyone should have cardkey *right now*
      - *Check this* – there isn't any form to fill out
    - Don't let others in (who knock)
      - Why, then, would we bother with cardkeys?
  - Computers
    - Standard EECS login forms (cs150-XY + password)
    - Logs into windows machines
    - Change your passwords (UNIX and Windows) ASAP
    - T.A.s will pass forms out after lab lecture *today*

Lab Policies (4)

- Lab Media
  - Printing
    - Three printers (A, B, C)
    - Computers will automatically print to nearest printer
    - Don't waste paper – this is Berkeley after all
  - Storage
    - C:/ – fast & volatile.
      - **Do**: Store/run temporary/[automatically generated] project files
      - **Don't**: Store code (it will get deleted upon logging out)
    - U:/ – slow & non-volatile.
      - **Do**: Store code (it won't get deleted)
      - **Don't**: Run the tools (they will run slowly)
    - SVN – submissions & project.
      - **Do**: Use in favor of U:/
      - **Don't**: Commit temporary project files (we've seen 600 GB of garbage)
      - *Will be setup shortly*

Lab Policies (5)

- Lab Design Platform
  - "XUPv5/ML505" (board)
  - LX110T-1 (FPGA)
  - New as of Spring 2009
  - Treat with extreme care!



- Our last board (CaLinx) lasted 8 years
- We'd like the XUPv5 to do the same*

* Fine print: if we catch you intentionally damaging the boards (penciling ICs, you name it), your lab access will be revoked and your standing put in jeopardy. This includes what your friends (who aren't in the class but who you have let into the lab) do to the boards. We have cameras!

Lab Policies (6)

- Lab Resources
  - Are the same as the class' resources
  - Website: http://inst.eecs.berkeley.edu/~cs150/sp10/
  - Newsgroup: https://inst.eecs.berkeley.edu/~webnews/webnews.cgi
  - Your T.A.s
  - Your peers
    - The T.A.s won't always be here (fact!)

Questions?

- Lab Lecture
  - Components
  - Expectations
- Lab Format
  - Components
  - Check-off
- Logistics
  - General lab policies
  - Lab {Usage, Access, Media, Platform, Resources}

FPGA Editor (1)

- What is FPGA Editor?

  "A graphical application for designing to & configuring FPGAs"

  – Design directly to the FPGA fabric

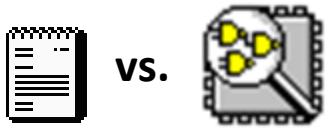
  – Very little CAD abstraction

    - No SPICE-like code (It's a GUI)

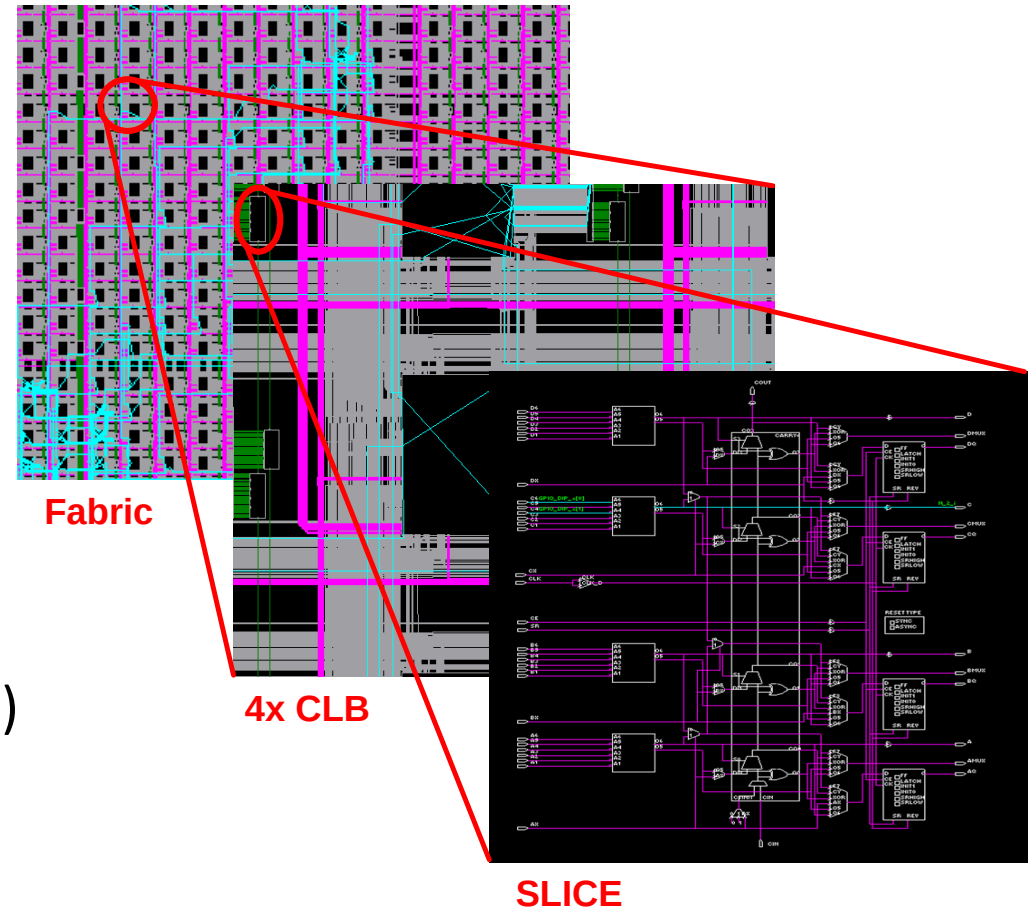
      → Just LUTs, SLICEs, CLBs, etc

  – FPGA Editor makes working with an FPGA roughly equivalent to working with a {proto, bread} board

FPGA Editor (2)



- Why bother?
  - In CS150
    - Introduction to FPGA architecture & hierarchy
  - In Industry
    - Design optimization
    - Debugging, Hard Macro IP
  - You will be working through an abstraction (Verilog HDL*) for much of the semester



* Hardware Description Language

FPGA Editor (3)

- Capabilities
  - Hand-route a design
    - Optimization, tuning
  - Faster debugging

    (1) Manually route a wire (or “net”) to a pin on the FPGA

    (2) Use an Oscilloscope/etc to probe the net
  - Bypass shortcomings of the embedded era
    - Old days: O-scope probe any signal you like
    - Modern days: Everything is embedded!

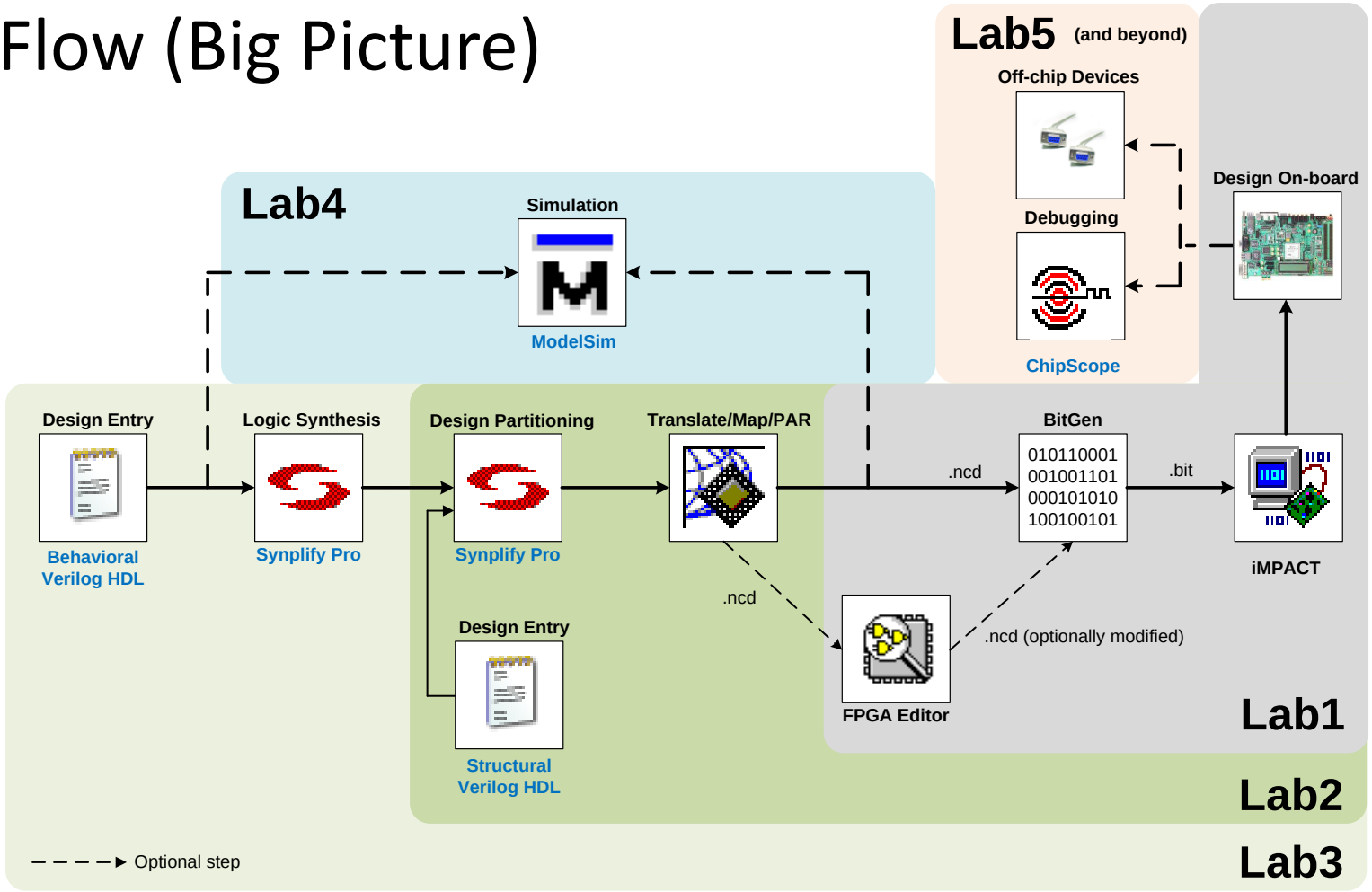
      → You can’t scope anything!

Lab 1 (1)

- Design with FPGA Editor
- You will learn how to…
  (1) Navigate the FPGA hierarchy
  (2) Program LUTs directly
  (3) Hand-route additional features into your design
- Explore a part of the CAD flow

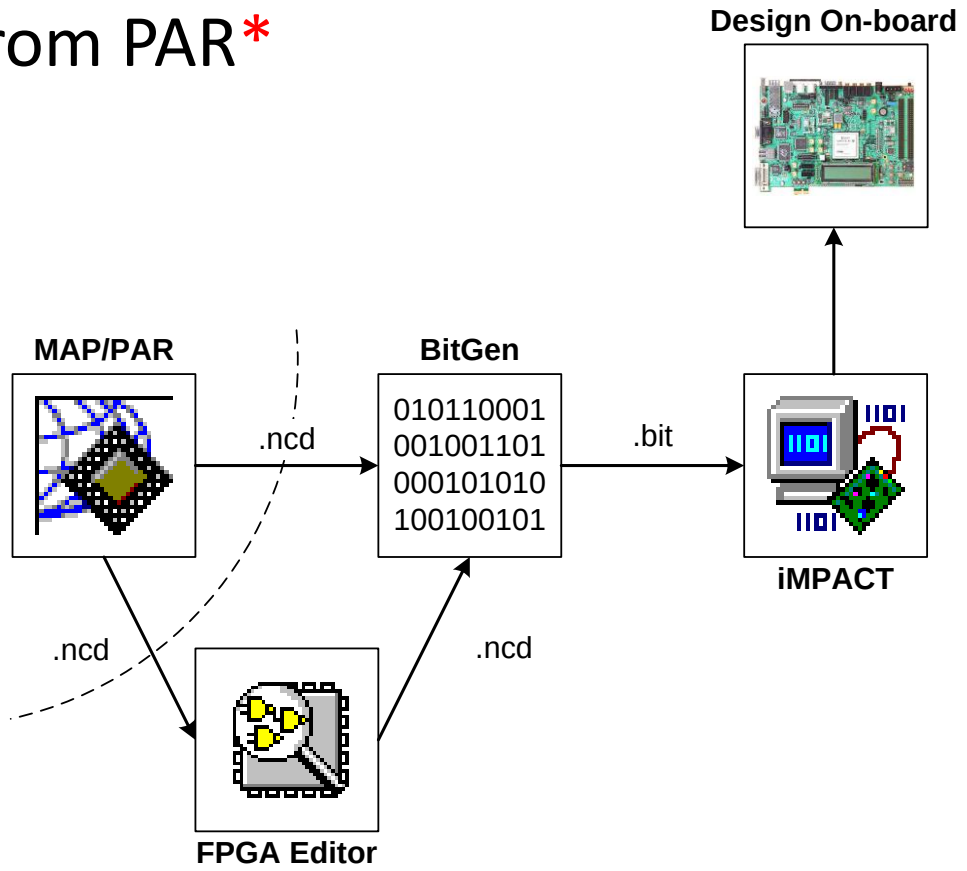
Lab 1 (2)

CAD Flow (Big Picture)



Lab 1 (3)

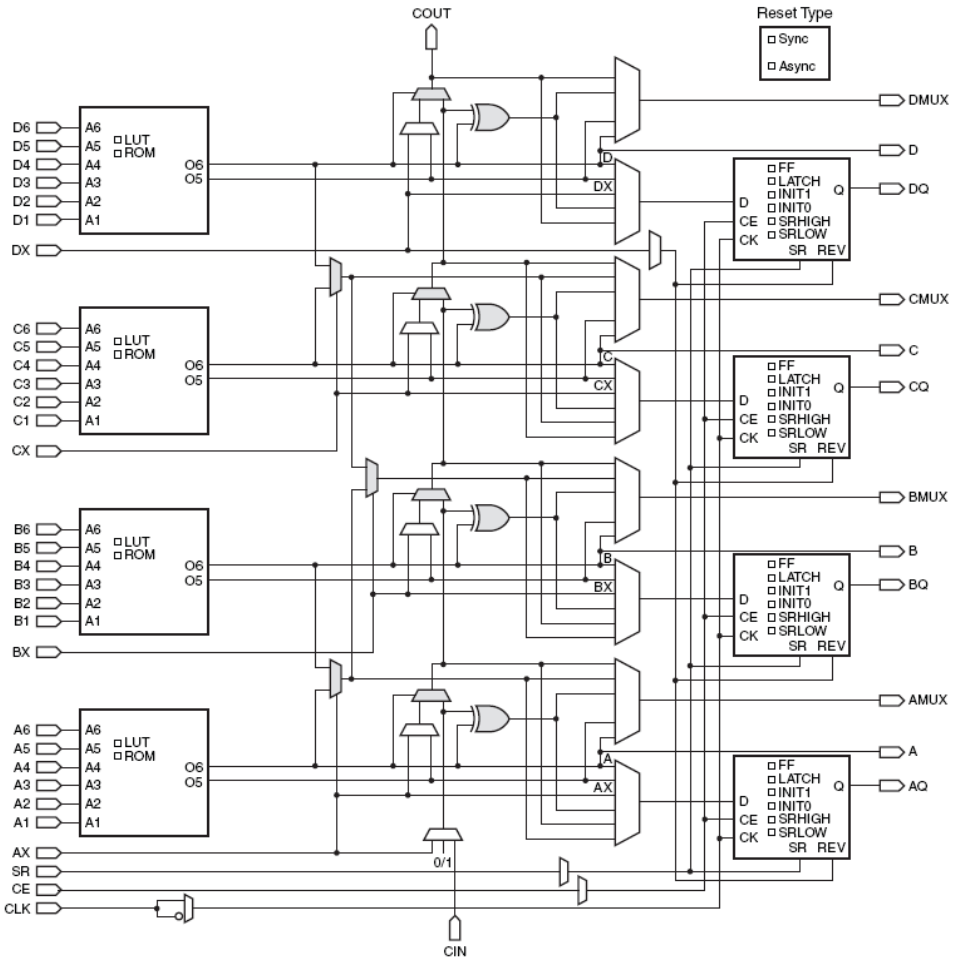
- CAD Flow (Lab 1)
  - We provide *.ncd files from PAR*
  - You will:
    (1) Modify the *.ncd
    (2) Generate a *.bit file
    (3) Program the FPGA



* PAR: Place and Route

Lab 1 (4)

- Pre-lab
  - Come to lab being able to understand this figure
  - This circuit is an FPGA building block
  - Every part of the lab is based on it
- Reading
  - ug190.pdf
    - Chapter 5



Virtex-5 SLICEL

Lab 1 (5)

- Come to lab having…
  (1) Read the lab document
  (2) Read the pre-lab material
- Be familiar with the following:
  - LUT
  - FPGA fabric
  - SLICEL vs. SLICEM
  - Architecture of the SLICEL
  - Configurable Logic Block (CLB)

Questions?

- FPGA Editor
- Lab 1
  - CAD flow
  - Pre-lab
  - Expectations

If you have questions after lab lecture, feel free to ask on the newsgroup!

Acknowledgements & Contributors

Slides developed by Chris Fletcher & John Wawrzynek (1/2010).

This work is based in part on slides by:

Chris Fletcher (2008-2009)

Greg Gibeling (2003-2005)

This work has been used by the following courses:

- UC Berkeley CS150 (Spring 2010): Components and Design Techniques for Digital Systems