

University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Homework Assignment 9: Ethernet; Circuit Timing
Due April 2nd, 2pm

Homework submissions must be made via the course SVN repository. Email submissions will not be accepted! Please format your homework as plain text, or PDF. You may use PNG for any necessary figures. Use a CAD program or neat scanned drawings for diagrams (Microsoft Visio is installed on the machines in 125 Cory).

1. Given a 10/100 Ethernet link operating at a line rate of 100Mb/s (Assume the producer is able to supply data at arbitrary high rates), how much time would a transfer of 10 million bytes of raw data take (no protocol embedded into the Ethernet frames)?

Assume that no inter-frame gap is needed, and “Jumbo” frames are disallowed.

2. You are an engineer at AcmeVideo, Inc. Your current display system has the following specifications:

- 30 frames/second
- black & white display (only one component for each pixel)
- 8 bits per pixel
- 600 pixels/line
- 600 lines/frame

The display system uses a frame buffer based on a SDRAM with the following specifications:

- 8-bit data interface
- $4+L$ cycles per read or write access, where L = burst length (consecutive memory accesses, 1 per cycle)
- Maximum $L = 6$
- 48 MHz clock frequency

Your marketing department would like to bring out a new product based on your current display system. It will have a display monitor that can be rotated 90 degrees and a mechanical switch to detect when the monitor is rotated. When the monitor is rotated, the display system must rotate the video output by 90 degrees to compensate. Your VP of engineering has decided that the cheapest way to achieve this compensation is to transform the image using the frame-buffer; it will be written to the frame buffer row-by-row, but read out column-by-column.

- (a) Using the existing frame buffer and changing the control logic, is it possible to support the rotation operation and maintain the display specifications? Show your work.

(b) Adhering to all other specs, what is the maximum display refresh rate when rotated?

3. **Before starting the problems below, please read sections 3.5.1-3.5.3 of DDCA.**

4. DDCA, Problem 3.30

5. DDCA, Problem 3.31

6. DDCA, Problem 3.32

7. Consider a CMOS AND gate implemented as a NAND gate followed by an inverter. Assume the inverter propagation delay is defined as follows (units in picoseconds):

$$\tau_p = 50 + 100 \cdot f$$

Where f is the fanout of the inverter, expressed in number of transistor gate inputs. For example, inverters contribute 2 to f and one input of a 2-input NOR gate contributes 2. **Note to people who have taken EE141: this is not the $f = \frac{C_{out}}{C_{in}}$ definition of fanout used in EE141.** Assume this inverter has the same propagation delay for both $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions.

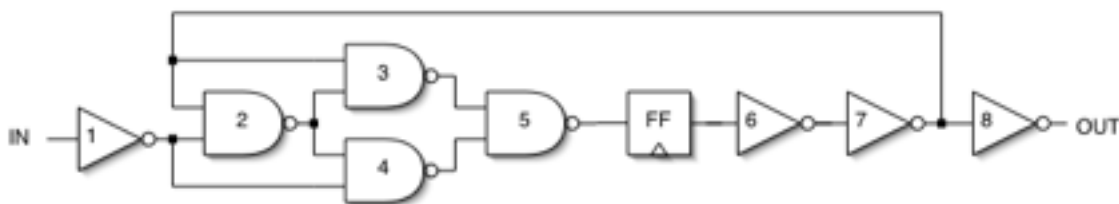
The NAND gate propagation delay is expressed as (in ps):

$$\tau_{p0 \rightarrow 1} = 100 + 75 \cdot f$$

$$\tau_{p1 \rightarrow 0} = 100 + 125 \cdot f$$

For the $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions, respectively. Write the expressions for the $0 \rightarrow 1$ and $1 \rightarrow 0$ propagation delays of the AND gate.

8. Consider the circuit shown here:



- The propagation delay (for both high-to-low and low-to-high transitions) of the inverters are $\tau_p = 50 + 100 \cdot f$ (in ps).
- The propagation delay (for both kinds of transitions) of the NAND gates are $\tau_p = 100 + 150 \cdot f$ (in ps).
- The flip-flop $t_{setup} = t_{clk-q} = 50ps$.
- There is no clock skew

- Assume there are three instances of this circuit cascaded together, we are focusing our analysis on the middle one.
- (a) Mark the critical path in the diagram
 - (b) List the gates of the critical path (by gate number) in the order of signal propagation and their associated delays. Remember to account for the fanout.
 - (c) What is the minimum clock period T for correct operation of this circuit?
9. You will need to look up a few numbers in “DC and Switching Characteristics” datasheet for the Virtex-5 family of FPGAs, pages 28-29. Assume a “-1” speed grade XC5V110T FPGA (same as on your boards in lab).
- Hint: look at the circuits measured in the table on pages 28-29. Think about the simplest implementation of these circuits.*
- (a) Using your familiarity with the Virtex 5 architecture, as well as the numbers in the datasheet, infer the smallest delay through the FPGA interconnect fabric.
 - (b) What is the delay through the O5 output of a Virtex 5 LUT? What about the O6 output?