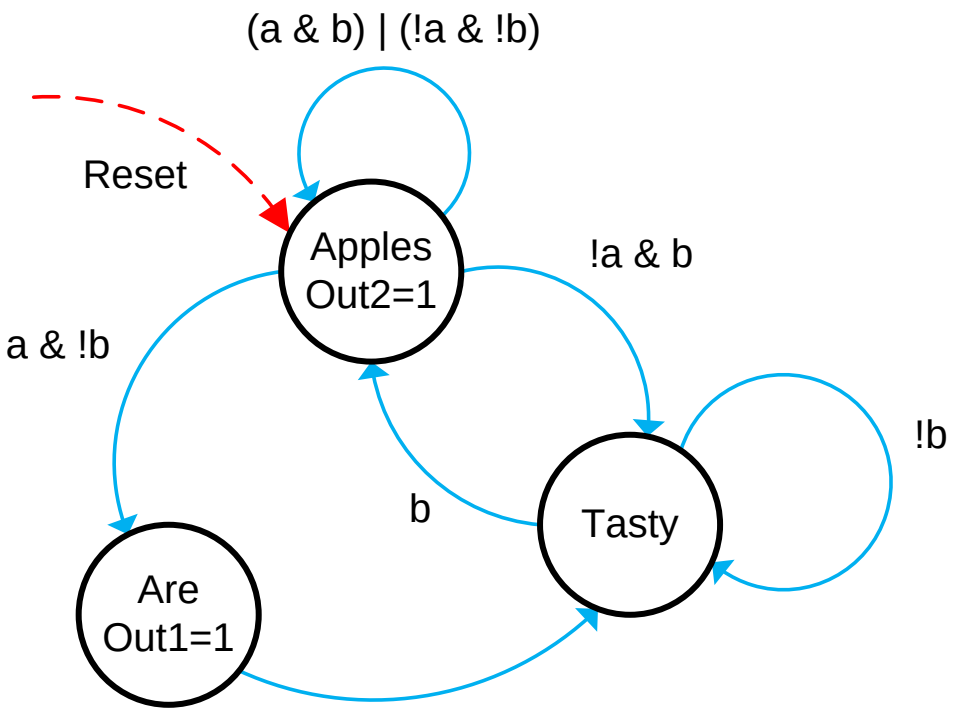
University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Homework Assignment 2: Testbenches, Transistors, and Implementation Technologies
Due February 19^{th}, 2pm

Homework submission will only be through SVN. Email submissions will not be accepted! Please format your homework as plain text with either PNG or PDF for any necessary figures. Microsoft Visio is installed on the machines in 125 Cory, and is a useful tool for drawing figures of all kinds.

1. (a) DDCA 4.44
   (b) In the context of a simulation testbench, what is a signal declared as a **reg** primarily used for?
2. DDCA 4.34
3. Shown here is a finite state machine like others that you have seen in this class:



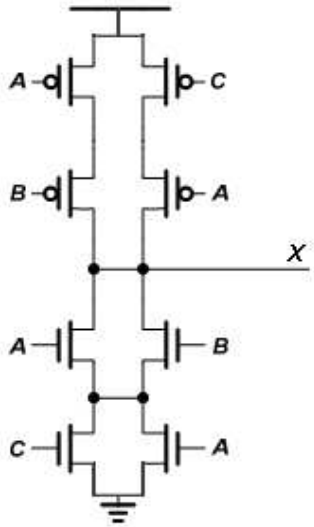
And here is a Verilog implementation of the state machine:

```
module TastyFSM (
    input reg   Clock,
    input reg   Reset,
    input reg   a,
    input reg   b,
    output reg  Out1,
    output wire Out2
);

localparam  APPLES = 2'd0,
            ARE = 2'd1,
            TASTY = 2'd2;

reg CurrentState, NextState;

assign Out2 = (CurrentState == APPLES);
assign Out1 = (NextState == ARE);

always@(posedge Clock) begin
    if (Reset) CurrentState = NextState;
    else CurrentState = APPLES;
end

always@( * ) begin
    case(NextState)
        APPLES : begin
            if (a & !b) NextState <= ARE;
            else if (!a & b) NextState = TASTY;
        end
        ARE : begin
            NextState <= TASTY;
        end
        TASTY : begin
            if (b) NextState <= ARE;
        end
    endcase
end

endmodule
```

As you may or may not have noticed, this Verilog is full of bugs. Please correct this Verilog so that it infers the state machine shown in the bubble-arc diagram.

4. DDCA 1.63

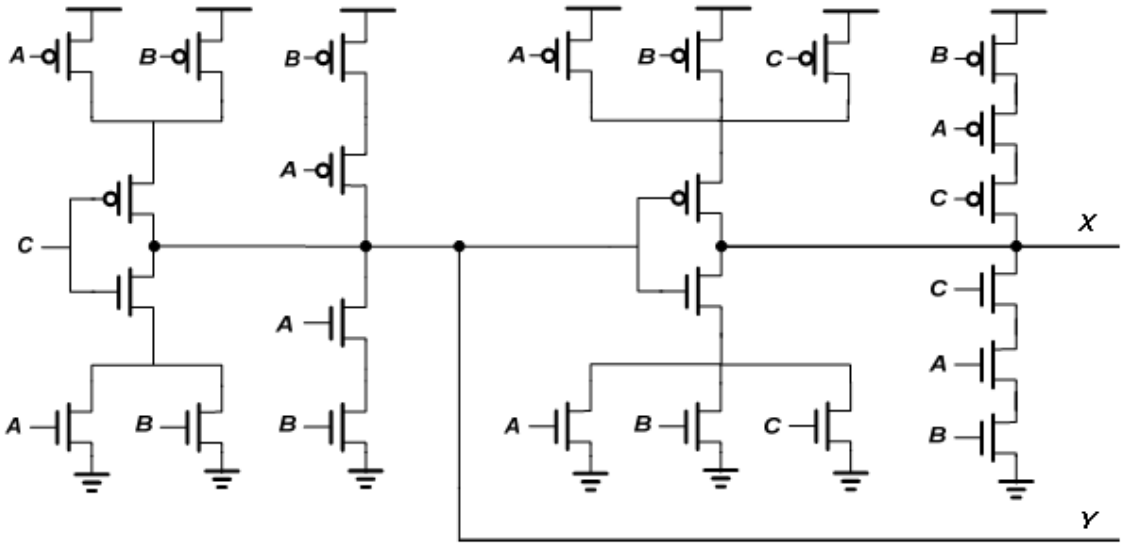
5. Given this circuit:



   (a) Write a truth table for the function performed by the gate shown. **A, B, C** are inputs and **X** is the output.

   (b) Is it possible to simplify this gate to reduce the number of transistors? If so, draw a simplified version.

6. Write the truth table for the function of this circuit:



   A, B, C are inputs, **X** and **Y** are the outputs.

7. Build the FSM in exercise 4.22 down to the level of transistors. Please draw your circuit diagram hierarchically (i.e. implement an **or** gate using transistors, then start using it in your main circuit).

8. In class we discussed a range of chip implementation alternatives: Full-custom, standard-cell, structured-ASIC, FPGA, GPP (general purpose processor). For each of these implementation alternatives, gauge the following metrics (i.e. "low time-to-market," etc):

   (a) NRE cost

   (b) Per-unit cost

   (c) Time-to-market

   (d) Application performance

   (e) Chip power consumption

9. Goto http://www.digikey.com and find one of the cheapest discrete Dual D flip-flop packages that you can find (you do not necessarily have to find the cheapest one, but it show be way under $1.00). To make sure that the part is not obsolete, please find one that is still stocked!

   (a) What is the cost of each flip-flop?

   (b) The Virtex-5 LX110T FPGA used in lab has approximately 70,000 flip-flops. Look up the cost for this part (you ARE searching for a XC5VLX110T part in a FF1136 package). How much would it cost to build the same number of flip-flops as an LX110T using the cheapest dual D flip-flop part that you found?

   (c) What is the cheapest Xilinx FPGA (not CPLD!) device that you can find on DigiKey? How many flip-flops does it have? To make sure the part is not obsolete, please find one that is still stocked! Hint: Consider looking up the "Spartan" family of FPGA devices.

   (d) Suppose you need a really cheap fix to a digital problem on a board that you ARE designing. For a very simple design with just a few flip-flops, discrete D flip-flop packages will be cheaper. What is the crossover point for which a Xilinx part will be cheaper?