University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Homework Assignment 2: FPGAs, LUTs and Basic Synchronous Digital Logic
Due February 5th, 2pm

Homework submission will only be through SVN. Email submissions will not be accepted! Please format your homework as plain text with either PNG or PDF for any necessary figures. Microsoft Visio is installed on the machines in 125 Cory, and is a useful tool for drawing figures of all kinds.

1. In this problem, we will investigate LUT partitioning against area and delay constraints. Consider the *and* gate reduction tree shown in Figure 1. You are given a box full of LUTs (ranging from 2 to 8 inputs). Each LUT costs $2^n + n$ area and n delay (where n is the number of inputs on the LUT). Partition the reduction tree into some combination of these LUTs in order to:

   (a) Minimize area.

   (b) Minimize delay.

   To answer each part, fill Figure 1 table cells with wire names to connect different wires (labeled $a0 \ldots a15$, $b0 \ldots b7$, $c0 \ldots c3$, and $d0 \ldots d1$) to different LUT inputs and outputs. You will not fill in every cell in the tables. Use only what you need.

2. Figure 2 shows a mystery circuit that has some output behavior given 3 inputs a, b and c. In parts 2b to 2e, this circuit can be thought of as the "black box" called *"Mystery."* In each part, you must construct the specified 1 or 2-input gate[1] using any number of *Mystery* blocks. You may connect each *Mystery* input to either a, b, c, logic 0 or logic 1. Try to use as few *Mystery* blocks as you can!

   (a) This circuit has a meaningful name − what is it? Feel free to use the provided truth table.

   (b) *and*

   (c) *or*

   (d) *not*

   (e) *xor*

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[1] Since you only need to construct a 2-input gate but have 3 inputs (a, b and c), the final output can be the specified logic function between any subset (of your choosing) of those inputs.
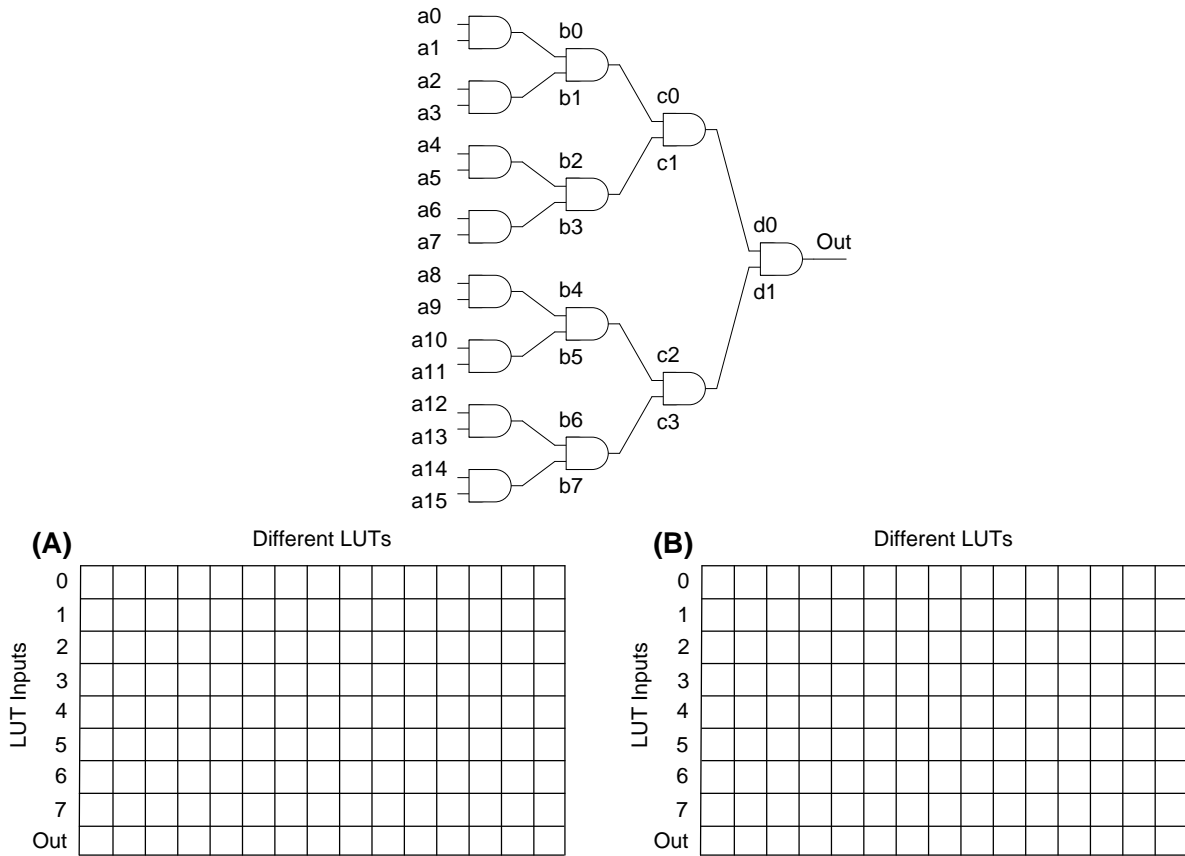
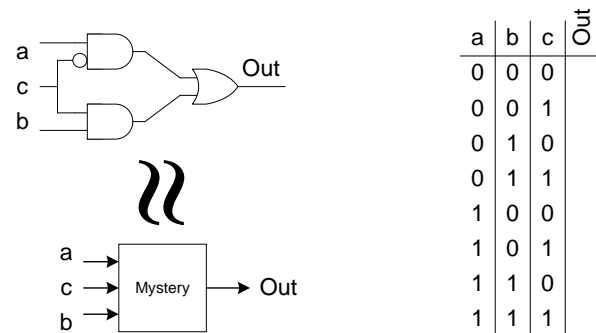Figure 1: An *and* gate reduction tree (Problem 1).
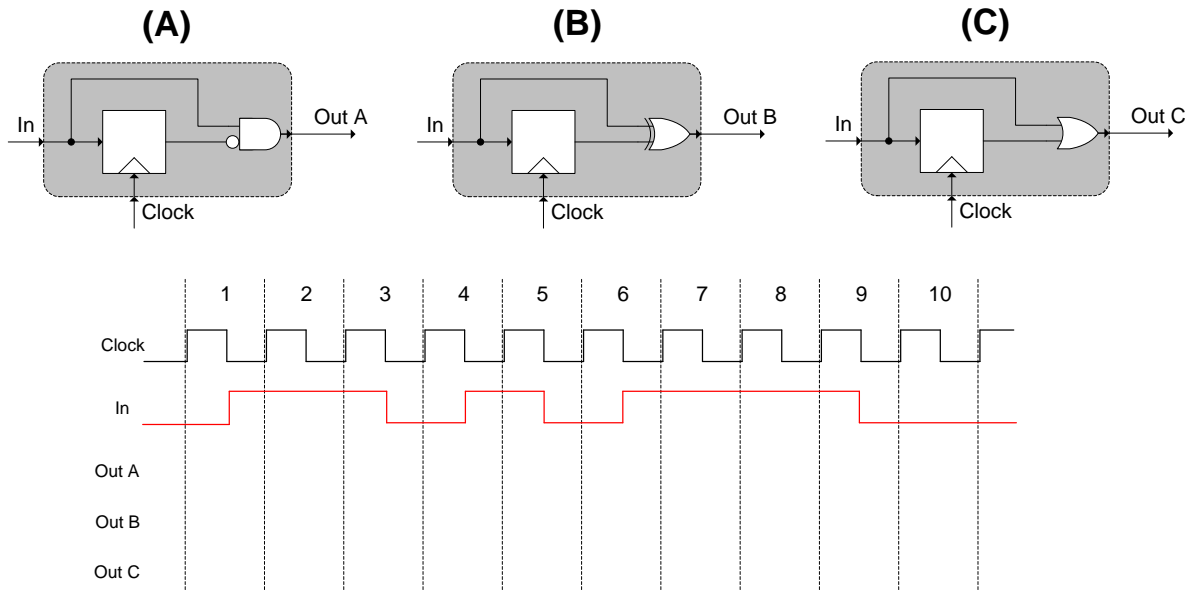

Figure 2: A mystery circuit (Problem 2).

Figure 3: A family of related circuits (Problem 3).

3. In this problem, you will explore how similar yet simple circuits can implement higher-level functions. Figure 3 shows a family of mystery circuits. For each of (i), (ii) and (iii), complete the following questions:

   (a) Complete the waveform diagram for the Out[2] port.

   (b) Look at the waveform relative to the input signal. Describe (in as few words as possible!) what this circuit does.

   (c) In Figure 4, allocate and route the components necessary to implement this circuit. *Note: You should implement all three circuits in the one SLICEL that is provided. Feel free to route SLICE outputs back to the SLICE inputs.*

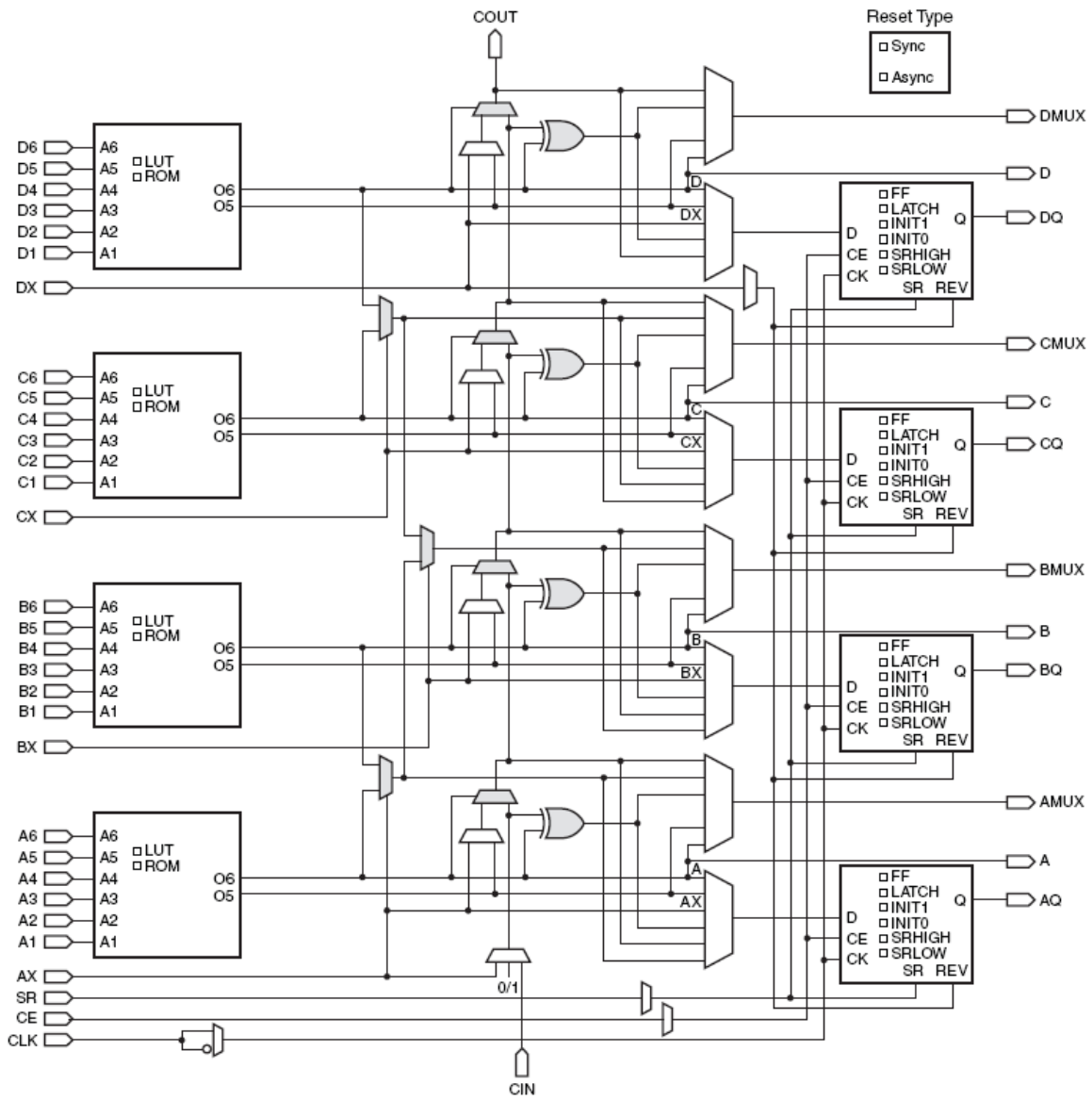[2]There is one incomplete waveform for each of the three circuits.

Figure 4: A Virtex-5 SLICEL (Problem 3).

4. Now that you have partitioned circuits into LUTs, you will practice partitioning a circuit into whole CLBs. A basic CLB is shown in Figure 5. Each CLB features a 4LUT, flip-flop and a mux to decide what input is connected to the flip-flop. Partition the circuit shown directly below the CLB in Figure 5 *into as few of these CLBs as you can.* You may connect each CLB input to a signal, logic 0, logic 1, or "*nc*" (for "no connection"). To answer the question, fill out the table at the bottom of Figure 5 using the same conventions that were used in Figure 4.

5. Thus far, this class has exposed you to the Virtex-5 LX110T FPGA. In this problem, we will study the SLICEM (shown in Figure 6) in a Spartan-3, an older Xilinx FPGA in the Spartan family. We provide only a reference figure for this problem, but a complete datasheet (much like *ug190.pdf*) exists for the Spartan. Information within this datasheet might be valuable (but is not necessary) in solving this problem. We encourage you to seek it out!

   (a) Unlike the Virtex-5, the Spartan is based on 4LUTs instead of 6LUTs. Based on Figure 6, how would you construct a 5LUT?

   (b) In class, we discussed how Virtex-5 SLICEMs can implement an $N : 1$ distributed RAM per 6LUT. As it turns out, the Spartan-3 has the same feature in its SLICEM. Given the dimensions of a Virtex-5 single-LUT distributed RAM cell, what are the dimensions of a Spartan-3 single-LUT distributed RAM cell?

   (c) You are given a choice between two imaginary FPGAs: one with $8\times$ Virtex-5 SLICEMs and another with $16\times$ Spartan-3 SLICEMs. Your design cannot fit into either FPGA right now because it uses too many LUTs. You notice, however, that a lot of the LUTs are spent implementing $2 : 1$ MUX functions. Given this information, which FPGA would you choose to implment your design? Why?
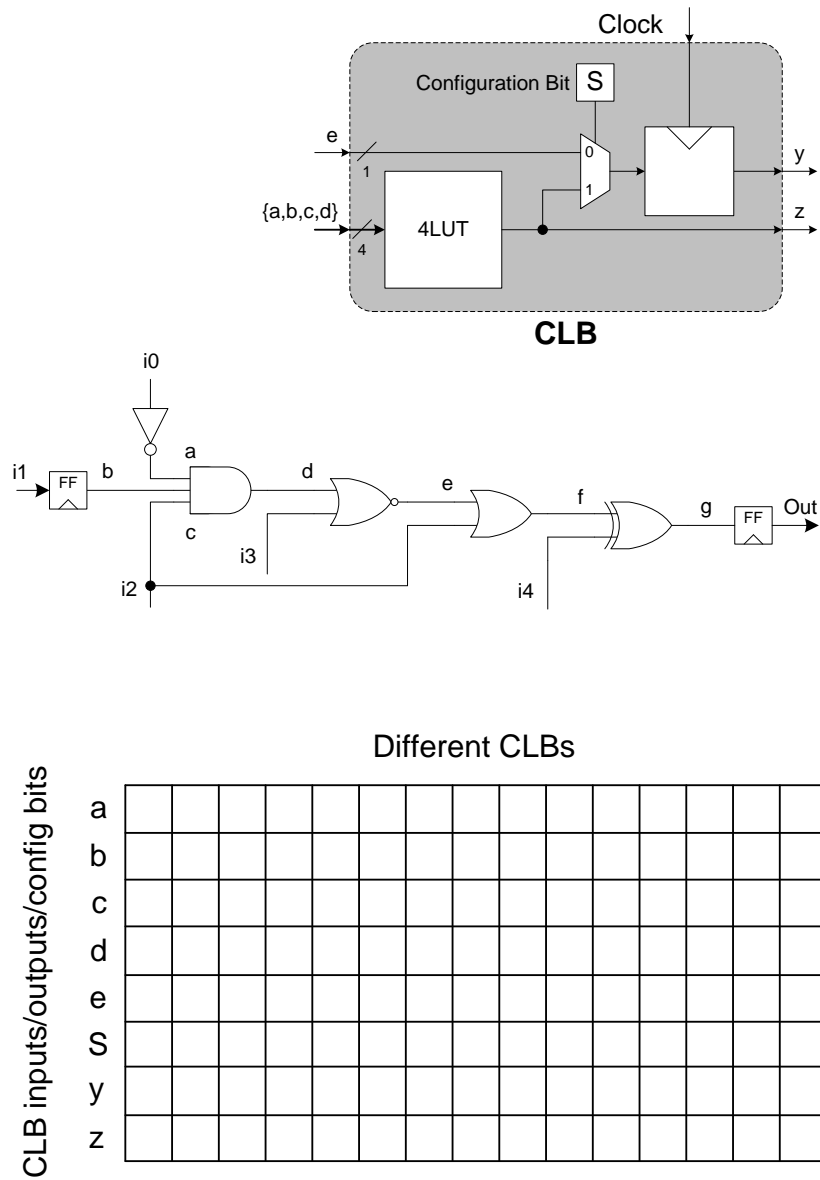
Clock

Configuration Bit S

e

1

{a,b,c,d}

4

4LUT

0

1

y

z

CLB

i0

i1

FF

b

a

c

d

i3

e

i2

f

i4

g

FF

Out

Different CLBs
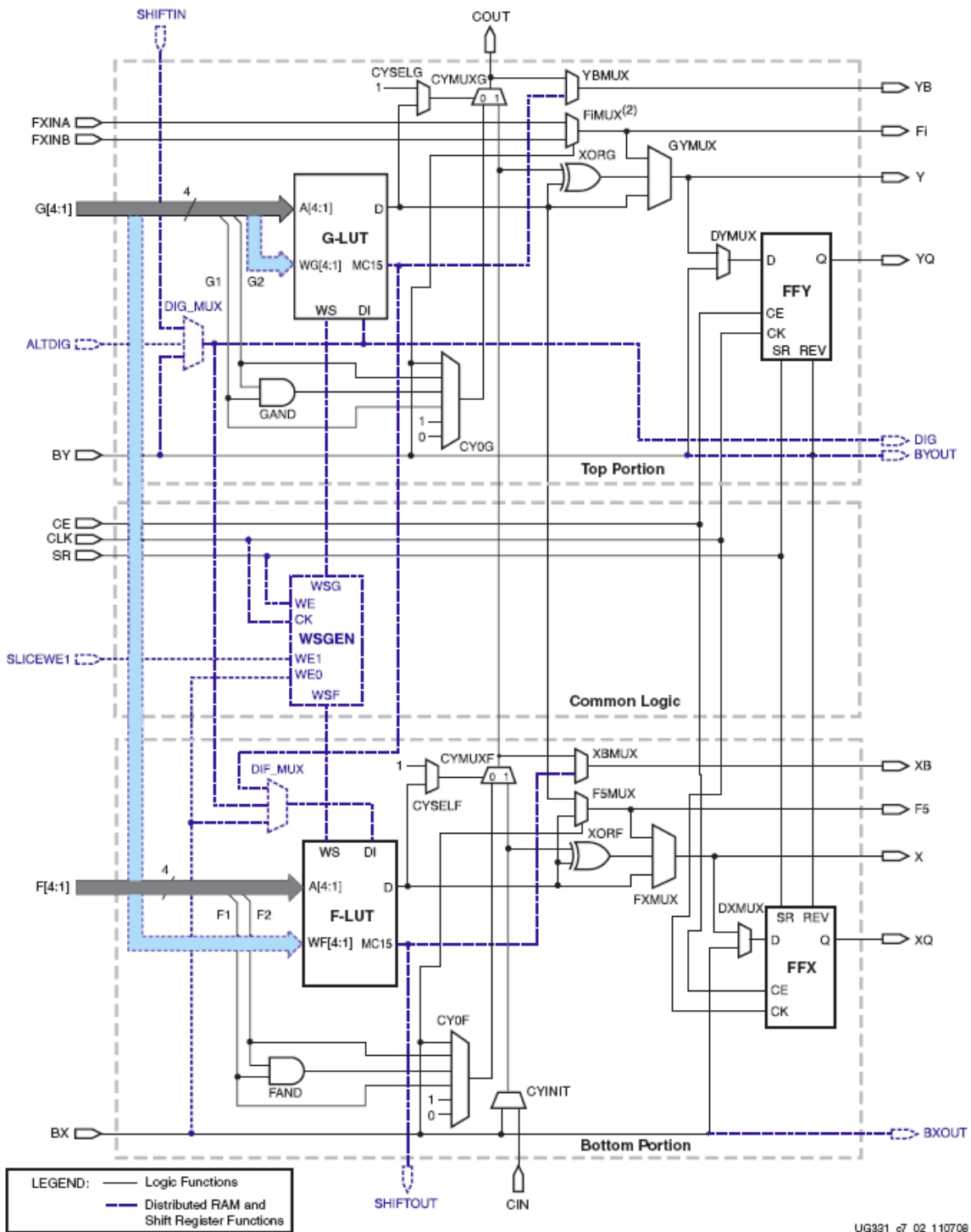
CLB inputs/outputs/config bits

a
b
c
d
e
S
y
z

Figure 5: Problem 4.

6

Figure 6: A Spartan-3 SLICEM (Problem 5).