EECS150: Homework 8, Power and Timing

UC Berkeley College of Engineering
Department of Electrical Engineering and Computer Science

1 Time Table

ASSIGNED	Friday, March 13^{th}
DUE	Friday, March 20^{th} at 2pm

Homework submission will only be through SVN. Email submissions will not be accepted!

1. You are given a static CMOS **6-input NAND** gate whose output is driving a capacitance $\mathbf{C_{load}}$. The gate is powered by a supply voltage $\mathbf{V_{DD}}$ and is part of a synchronous circuit running at some frequency **f**. Ignore any static (leakage) currents for this problem.

   (a) As a function of the given variables, how much energy is dissipated by the circuit each time the output makes a $0 \rightarrow 1$ transition? What about a $1 \rightarrow 0$ transition? Is any energy used if the output stays the same?

   (b) As a function of the given variables, what is the average power dissipated by this circuit if, on any given cycle, the probability that the output will make either a $0 \rightarrow 1$ or $1 \rightarrow 0$ transition is α?

   (c) Suppose each **input** has a 50% chance of switching (either a $0 \rightarrow 1$ or $1 \rightarrow 0$ transition) each cycle. Find a numerical value for α, the probability that the output of the gate switches on any given cycle.

   (d) Let $\mathbf{C_{load}} = 100fF$, $\mathbf{V_{DD}} = 1.2V$, and $\mathbf{f} = 2GHz$. Using the α you found in the previous part, numerically calculate the average power dissipated by this gate.

   (e) Suppose instead that we were analyzing a **6-input XOR** gate being subjected to the exact same conditions. Would you expect its average power consumption be bigger, smaller, or equal to that of the **6-input NAND** gate? Why?

2. Your boss at **chipsRus.com** asks you to determine the average node activity factor α of a particular chip. In the lab you find:

   - A power supply for powering the chip at some particular voltage **V**.
   - A clock generator to output some frequency **f**.
   - A current meter for determining its average current consumption while running **I**.
   - A pattern generator for applying typical input patterns to the chip while running.

   Additionally you:

   - Call up the designer of the chip and leave voice mail asking her the number of internal nodes in the chip **n**.
   - and the average node capacitance **C**.

   (a) Derive a formula you can use for finding α.

(b) The designer calls back and says that the chip has 1 Million nodes, and each node has an average capacitance of **10fF**. You go to the lab and measure the average current consumption to be **0.25 A** at **2 V** and **100 MHz**. What is the value of α?

(c) Suppose you turn off your clock generator and find that the circuit is still drawing a hefty **0.10 A** at **2 V**. Explain what is happening and modify the activity factor α that you found earlier to account for this.

3. Consider a CMOS AND gate implemented as a NAND gate followed by an inverter. Assume the inverter propagation delay is defined as follows (units in picoseconds):

$$\tau_p = 50 + 100 \cdot f$$

Where **f** is the fanout of the inverter, expressed in number of transistor gate inputs. For example, inverters contribute 2 to **f** and one input of a 2-input NOR gate contributes 2. **Note to people who have taken EE141: this is not the $f = \frac{C_{out}}{C_{in}}$ definition of fanout used in EE141**. Assume this inverter has the same propagation delay for both $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions.

The NAND gate propagation delay is expressed as (in ps):

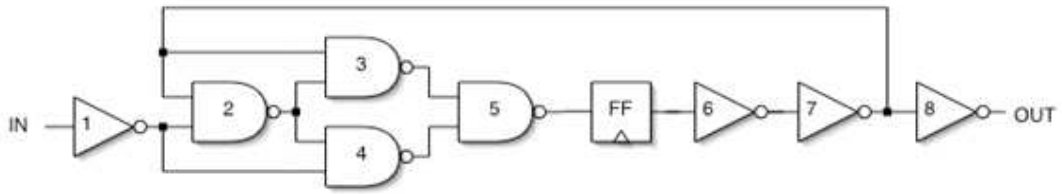
$$\tau_{p0\rightarrow1} = 100 + 75 \cdot f$$

$$\tau_{p1\rightarrow0} = 100 + 125 \cdot f$$

For the $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions, respectively. Write the expressions for the $0 \rightarrow 1$ and $1 \rightarrow 0$ propagation delays of the AND gate.

4. Consider the circuit given in Figure 1.

Figure 1 Interesting Circuit



- The propagation delay (for both high-to-low and low-to-high transitions) of the inverters are $\tau_p = 50 + 100 \cdot f$ (in ps).
- The propagation delay (for both kinds of transitions) of the NAND gates are $\tau_p = 100 + 150 \cdot f$ (in ps).
- The flip-flop $t_{setup} = t_{clk-q} = 50ps$.
- There is no clock skew
- There are three instances of this circuit cascaded together, we are focusing our analysis on the middle one.

(a) Mark the critical path in the diagram

(b) List the gates of the critical path (by gate number) in the order of signal propagation and their associated delays. Remember to account for the fanout.

(c) What is the minimum clock period **T** for correct operation of this circuit?

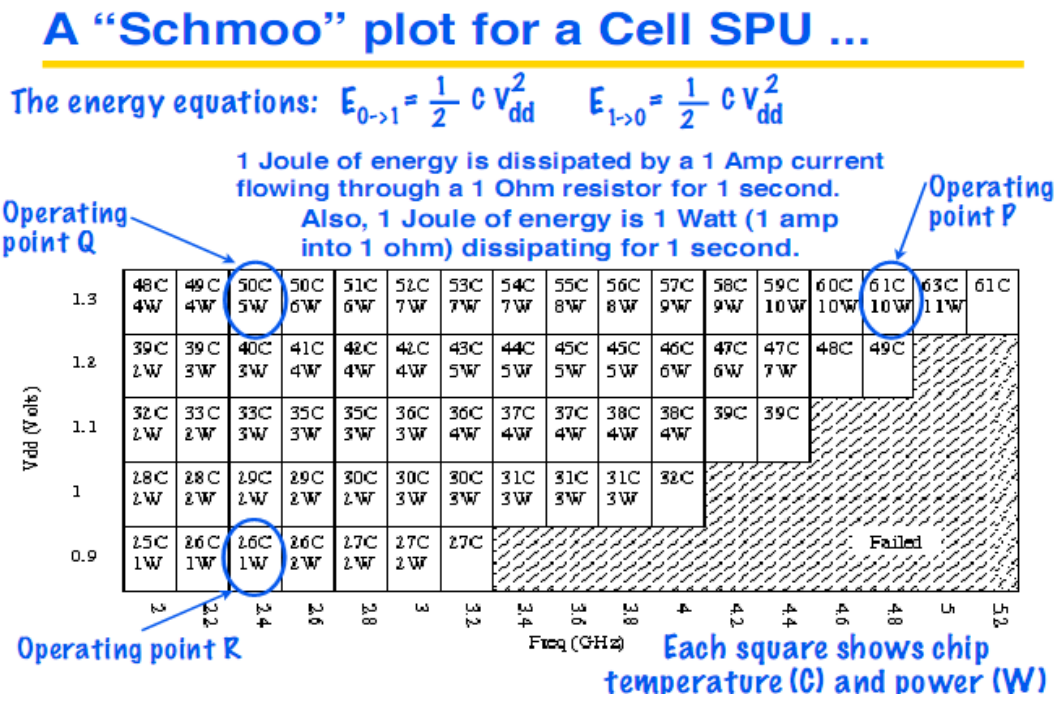
5. Consider an **n-bit ripple-carry adder** implemented using the full-adder circuit given in DDCA **Figure 4.8**.

(a) Find the critical path through this adder and the input combination that triggers it.

(b) Count the number of gate delays (i.e. if a signal passes through an XOR gate, add 1 to its gate delay) in the critical path as a function of **n**.

6. Figure 2 shows a Schmoo plot for a processor.

Figure 2 Schmoo plot of a processor



In this problem, the processor characterized by the Schmoo plot is used in a system along with support components that use K Watts of power. For example, in a laptop, the support chips might consume 2 Watts. For this system, K = 2.

When the processor is running, the support components must stay on. A CPU instruction may be used to turn the processor and the support components off. When off, the processor and the support components both use no power at all.

(a) Different systems may have different values of K. For example, the support chips for a laptop design may consume 2 Watts (K = 2), while support chips for a desktop design may consume 7 Watts (K = 7).

A program runs twice as fast at Operating Point P (shown in Figure 2) than at Operating Point Q. The last instruction of the program turns off power to the processor and its support chips.

i. For what range of values for K does Operating Point P use the lowest amount of energy to run the program?

ii. For what range of values for K does Operating Point Q use the lowest amount of energy to run the program?

iii. For what range of values for K do Operating Points P and Q use the same amount of energy?

(b) A program runs twice as fast at Operating Point P than at Operating Point R. The last instruction of the program turns off power to the processor and its support chips.

i. For what range of values of K does Operating Point P use the lowest amount of energy to run the program?

ii. For what range of values of K does Operating Point R use the lowest amount of energy to run the program?

iii. For what range of values for K do Operating Points P and R use the same amount of energy?