EECS150: Homework 5, Transistors, Single-cycle MIPS Processor

UC Berkeley College of Engineering
Department of Electrical Engineering and Computer Science

1 Time Table

ASSIGNED	Friday, February 20^{th}
DUE	Friday, February 27^{th} at 2pm

Homework submission will only be through SVN. Email submissions will not be accepted!

1. Draw the circuit diagram for a 2:1 Multiplexer using only 6 transistors.
2. Draw the circuit diagram for a positive level sensitive latch using only inverters, and tri-state buffers.
3. Draw a transistor-level diagram showing all the details of a negative edge-triggered flip-flop. Your circuit should have only two inputs, **clk** and **d**, and two outputs, **q** and $\overline{\mathbf{q}}$.
4. Draw a transistor-level circuit diagram for a switching circuit with two data inputs **x0** and **x1**, one control input **cross**, and two outputs **y0** and **y1**, with the following function:

   ```
   if (cross == 1)then y0 = x1, y1 = x0 else y0 = x0, y1 = x1
   ```

5. Build the FSM in exercise 4.22 down to the level of transistors. Please draw your circuit diagram hierarchically (i.e. implement an OR gate using transistors, then start using it in your main circuit).
6. Consider the single-cycle MIPS processor presented in lecture this week. Remember, it executes only the small set of the complete MIPS instruction set: **add**, **sub**, **or**, **slt**, **lw**, **sw**, **beq**.

   Assume that it has 1K words of instruction memory and 1K words of data memory. The instruction memory can hold any sequence of valid instructions. Suppose we want to describe this processor as an FSM (i.e. draw out a state transition diagram). How many state bubbles are in the STD? Note: don't bother to actually draw the STD.
7. DDCA 7.3, all parts
8. DDCA 7.4
9. DDCA 7.10, **just do this for 7.3a and 7.3b**