EECS150: Homework 6, MIPS Processor, RAM

UC Berkeley College of Engineering
Department of Electrical Engineering and Computer Science

1 Time Table

ASSIGNED	Saturday, February 28^{th}
DUE	Friday, March 6^{th} at 2pm

Homework submission will only be through SVN. Email submissions will not be accepted!

1. DDCA 8.24
2. Given two **256 x 32 single-port** RAMs, construct a **256 x 32 simple dual-port** RAM. You are allowed to use any additional gates, multiplexers or flip flops, but are limited to a total of 256 1-bit flip flops. Draw the schematic.
3. Given four **1k x 16 simple dual-port** RAMs, construct a **4k x 16 simple dual-port** RAM. You are allowed to use any additional gates or multiplexers. Draw the schematic.
4. For this section, you will be taking another look at LUTs.
   (a) Implement a basic 4-input LUT down to the transistor level. Allow the LUT to be programmable with a new function whenever the `prog` signal is asserted. How many configuration bits does your LUT need?
   (b) Modify your basic 4-input LUT such that it may also be used as a **16 x 1 Simple Dual Port RAM** (with synchronous writes) whenever the configuration bit `ram` is set. It should take `WriteEnable, WriteAddress, DataIn, Clock` as additional inputs. Draw the schematic of the new circuit down to the level of transistors.
   (c) Modify the new 4-input LUT such that it can also be used as a 16-bit shift register whenever the configuration bit `shift` is set.
5. Using the Block RAM section of the Virtex-5 datasheet as a reference, **roughly estimate** the number of transistors it will take to implement a 36k Block RAM on the Virtex-5. Clearly explain and justify the number you came up with. (Hint: some factors you may wish to consider are width, depth, number of ports, etc.)
6. Consider the circuit pictured in Figure 1.
   (a) Complete the timing diagram in Figure 2 for the circuit. Note that it may be helpful for you to think about the inverters as having a little bit of delay. What does this circuit do if `X` is 0 and `Y` is 1? Why?
   (b) How would the waveform for signal `E` change if the circuit had 5 inverters in series instead of 3? Why?
7. **Come prepared for design review during your lab section!**

Figure 1 A weird circuit

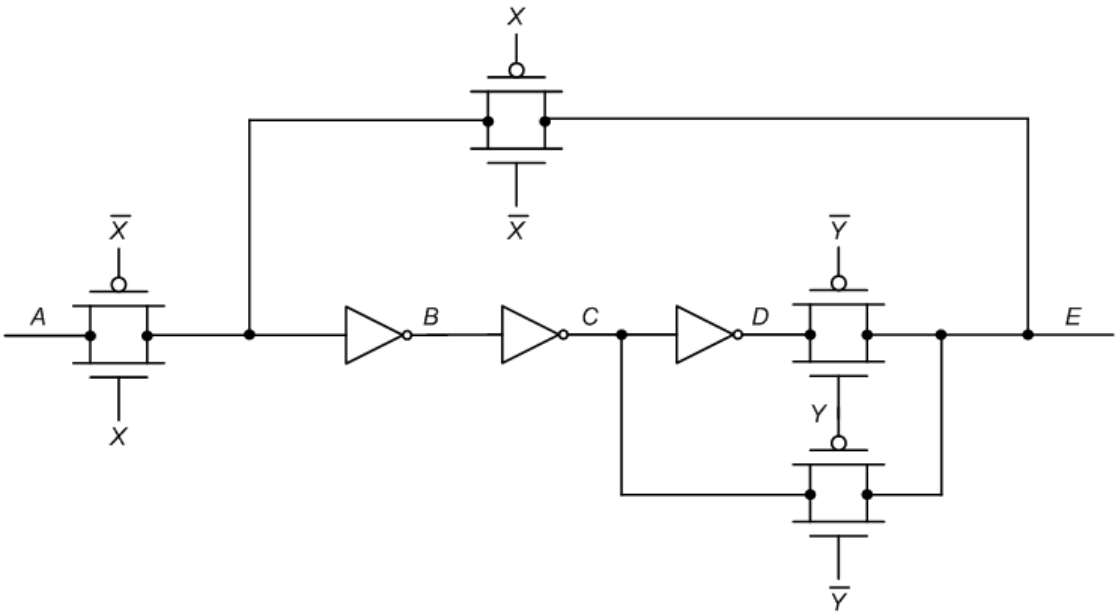

Figure 2 Timing Diagram for the weird circuit