University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Discussion 3: More Verilog and some CMOS

Feb 12, 2010

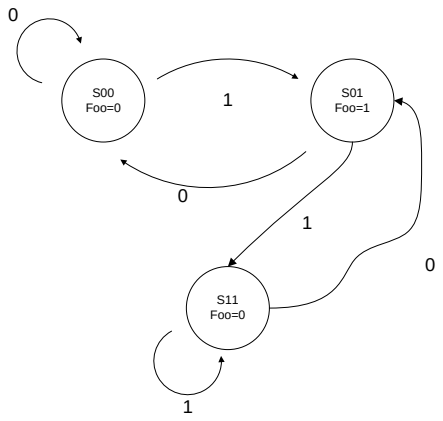
Brandon Myers

1. Write a Verilog module, Duplicate, that takes an input signal In and passes it thru to every bit of the output signal Out. Out is N bits wide; N is a parameter.

2. Write a Verilog module for a level sensitive latch, with interface In, Out, and C ("clock"). It must have a parameter Level, which if 1 makes the latch sensitive to high and if 0 makes the latch sensitive to low.

3. Design a 4:16 decoder out of 2:4 decoders and 2-input gates. Draw the circuit.

4. Consider the FSM state-transition diagram below.



   Write a Verilog module to implement this FSM.

5. A gray code counter is like a binary counter except with a different encoding, where every adjacent output changes just one bit. For example a sequence for a 2-bit gray code counter is
   00
   01
   11
   10
   Come up with a 3-bit gray code sequence and write a Verilog module, GrayCodeCounter, which is a gray code counter with this sequence.

6. State machines and FPGAs.

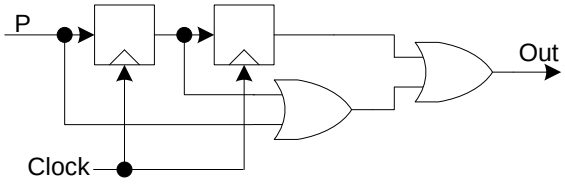
   (a) What is the minimum number of bits of state required to implement an FSM with 6 states?

(b) I wrote my FSM module in Verilog so that each of the 6 states had a unique binary encoding. But when I ran synthesis on the module, the RTL schematic shows 6 flipflops.

i. What's going on?

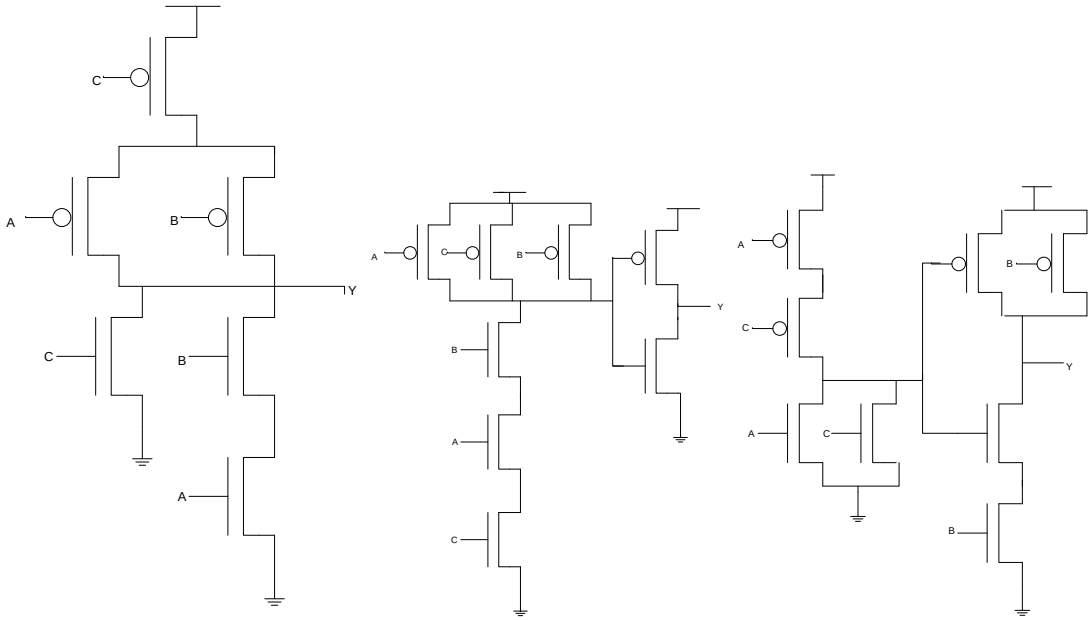
ii. Why would the synthesis tool do this?

7. Write a Verilog module for the following circuit:



8. What is CMOS?

9. Give the boolean equation implemented by each of the CMOS circuits (input A,B,C; output Y).



10. Design a 2-input XOR in CMOS.