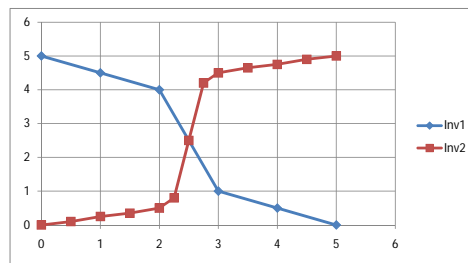


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Discussion 1 Solutions
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1. (a) See below



(b) See below

In	Out
0	0
1	1

(c) Schematic is that of an inverter without the dot at the tip. “buffer”

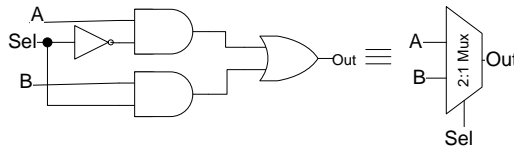
(d) Yes, the buffer is useful. Although its logic function is identity, it can restore a signal. It also has better noise margins than a single inverter. Series of inverters are used to reduce delay by driving large capacitances using successively larger gates, reduce delay by cutting the length of wires (RC line delay is proportional to length squared), driving signals across the chip or off chip.

2. Feed the same inputs[1:0] into two 2-input LUTs. The outputs go into a 2:1 Mux, whose output is the output of the 3-LUT. The last input bit, input[2], will be the mux select. This can be illustrated with truth tables.

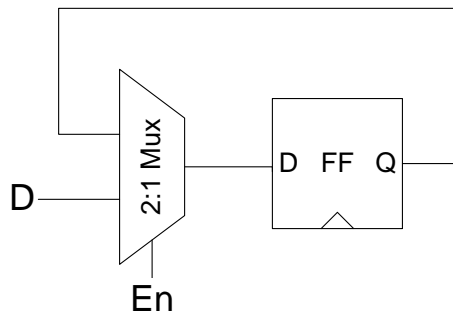
C	A	B	Y
0	0	0	F(0,0,0)
0	0	1	F(0,0,1)
0	1	0	F(0,1,0)
0	1	1	F(0,1,1)
1	0	0	F(1,0,0)
1	0	1	F(1,0,1)
1	1	0	F(1,1,0)
1	1	1	F(1,1,1)

Notice that the top half of the truth table, as written, has $C=0$ for all entries. The bottom half of the truth table has $C=1$ for all entries. This third input C can be the mux select that chooses the top half of the truth table or the bottom half. Each of the 2LUTs, with inputs A and B , can implement the respective half of the truth table, and the output of the 3LUT is chosen by C .

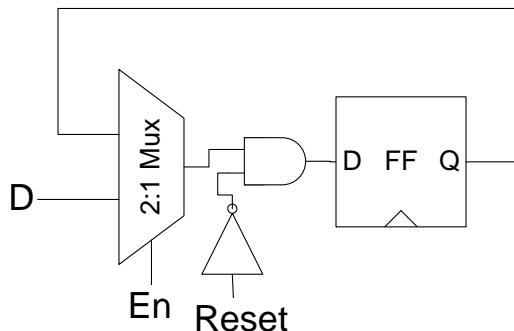
3. Outputs a 1 if the current input is different from the previous cycle's input. "Previous cycle's input" here means the value of In at the last rising edge of the Clock.
4. (a) See below



- (b) Use a feedback loop so that when Enable is low, the value stored by the FlipFlop is captured again. When Enable is Hi, the Input will pass through.



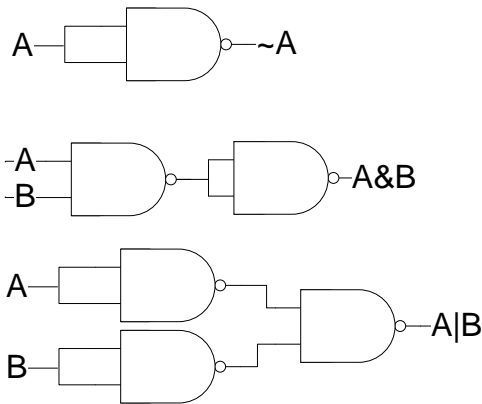
- (c) See below



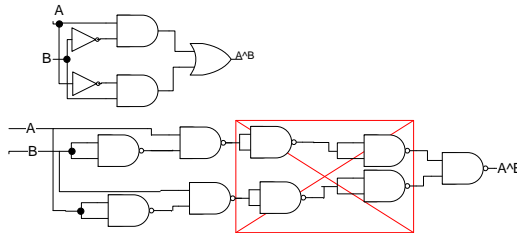
When Reset is high, it makes the AND gate always output a 0, which will make the FlipFlop capture a 0 on the next rising edge of the Clock. This is synchronous Reset, because the reset happens at the clock edge and the reset will only occur if Reset is high at the clock

edge (even if it went high during the clock cycle and then back to low). In contrast, if the FlipFlop reset as soon as Reset goes high, then this is asynchronous reset (also called “Clear”).

5. (a) Yes, 2-input NAND and 2-input NOR are gates that can alone build any boolean function.
- (b) To prove the claim, we can use the given statement that AND, OR, and NOT can build any boolean function. So, if we build these three gates from NAND (or NOR) then we have proven the statement in (a).



- (c) Notice that the boolean equation for XOR is $A * B + A * \sim B$. From this, the basic implementation AND, OR, NOT can be built. To directly get an XOR design in NAND gates, just replace each gate with its NAND gate implementation.



Notice that two sets of inverters cancel out, to give a 5-NAND implementation of XOR. It turns out that a 4-NAND implementation is actually possible, with more thought.

Try the NOR gate version of these problems!